

Design Tips Bruce Archambeault, Associate Editor

elcome to Design Tips! In this issue I revisit the subject of return current flow and inductance and continue on a Design Tip from a few issues ago. Inductance remains a topic of discussion and debate, and I have found that very few people truly understand inductance! Whenever I think I have the subject mastered, I speak to someone like Dr. Albert Ruehli or Professor Clayton Paul and realize that I need to learn more! So I encourage all readers to always be open to learning new things and improving their understanding of the fundamentals of our 'science'.

Please send me your most useful design tip for considera-

tion in this section. Ideas should not be limited by anything other than your imagination! Please send these submissions to bruce.arch@ieee.org. I look forward to receiving many "Design Tips!" Please also let me know if you have any comments or suggestions for this section, or comments on the Design Tips articles.

You will also find "Design Tid-Bits" at the end of the Design Tips article. These Tid-Bits are intended to be a very short description of EMC design best practices and cover a wide range of EMC design issues. Please send your contributions to bruce.arch@ieee.org.

PART II Resistive vs. Inductive Return Current Paths

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n the Spring 2008 Issue #217 of this Newsletter, I wrote a Design Tip concerning the path low frequency current and high frequency current take, and provided some (simple) formulas. While the formula I published in this Newsletter article works fine for the low frequency case in the original article, it is not valid for high frequencies since the microstrip and return path (in the plane beneath the microstrip) are extremely closely coupled. There is a much better way to estimate this high frequency inductance. This article will update the results from the previous article.

The main point of the article, that the return current will always follow the path of least *impedance*, remains valid! At lower frequencies, this means the path of least *resistance* and at high frequencies this means the path of least *inductance*. The change over frequency can be surprising low. The calculation of this change over frequency is not difficult from a first-order engineering accuracy point of view.

U-Shaped Printed Circuit Board (PCB) Trace

The same simple example is used to illustrate the change over frequency calculation can be obtained using a simple microstrip trace over a ground-reference plane on a PCB. Naturally, non-PCB examples are also valid.

Figure 1 shows a microstrip over a reference plane, and the dimensions for a U-shaped trace. The source is at one end and the load is at the opposite end of this U-shaped trace. At very low frequencies, it is expected the return current will go straight across from the load to the source without traveling under the microstrip trace. At very high frequencies, it is expected that the large loop area formed by points $A \rightarrow B \rightarrow C \rightarrow D \rightarrow A$ will have very high impedance and the return current

will return under the trace. Even though the path for the return current under the trace is longer than the low frequency path, the loop area is smaller, hence the inductance (and impedance) is lower with the path $A \rightarrow B \rightarrow C \rightarrow D \rightarrow C \rightarrow B \rightarrow A$.

Low Frequency Inductance Calculation

The low frequency inductance of these two paths can be calculated using a rough approximation¹ from the rectangular inductance formula given in equation (1) [1]. This formula is based on the Biot-Savart Law. While this formula looks intimidating at first, it is actually fairly simple to program into a spreadsheet, etc. When using this formula, we calculate the inductance of the shorter path (low frequency path) to be 733 nH. This is based on a 9" x 4" rectangle, where the conductor size = 10 mils (the width of the trace)².

High Frequency Inductance Calculation

The high frequency inductance assumes the current will flow in the plane beneath the microstrip. There are a number of 2-D field solvers commercially available, as well as quick calcu-



Trace total Length = 22"

Trace is 10 mils wide, 1 mil thick, 10 mils above GND plane

Figure 1. Physical Geometry, For Example

¹ This is the same formula from original article.

² This is a very crude estimate, since equation (1) assumes a round conductor.

lators, to find the per-unit-length parameters of a simple microstrip. One such simple calculator [2] was used to find the impedance for this microstrip structure equal to 106.1 ohms (using air dielectric). Using equation (2) and the resulting capacitance of 0.853 pF/in, the per-unit-length inductance is 9.6 nH/in. Therefore, using this approach results in the 22" trace with a total loop inductance of 211 NH.

$$A = h \ln\left(\frac{h + \sqrt{h^2 + w^2}}{w}\right)$$

$$B = w \ln\left(\frac{w + \sqrt{h^2 + w^2}}{h}\right)$$

$$C = h \ln\left(\frac{2h}{a}\right) + w \ln\left(\frac{2w}{a}\right)$$

$$L = \frac{\mu_0}{\pi} \left(-2(w+h) + 2\sqrt{h^2 + w^2} - A - B + C\right)$$
(1)

where

w = the width of the rectangle (wide dimension) h = the height of the rectangle (short dimension), and a = the wire radius.

$$Z_{0} = \frac{87}{\sqrt{\varepsilon_{r} + 1/41}} \ln\left(\frac{5.98H}{0.8W + T}\right) ohms$$

$$C_{0} = \frac{0.67(\varepsilon_{r} + 1.41)}{\ln\left(\frac{5.98H}{0.8W + T}\right)} pF / inch$$

$$Z_{0} = \sqrt{\frac{L_{0}}{C_{0}}}$$
(2)

Where: H = thickness of dielectric T = thickness of microstrip conductor W = width of microstrip conductor *Valid for* 0.1 < W/H < 3.0

Accurate Inductance Calculation

As engineers, we naturally strive for accuracy in our calculations. This lead me to use an IBM internally developed computational electromagnetic calculation code called Power-PEEC, which is based on the Partial Element Equivalent Circuit (PEEC) technique. The previous high frequency calculations (based on 2-D solvers) are reasonably accurate, but the low frequency calculations are somewhat crude, since the conductor shape is different than the simple equation assumption, as well the return current path between points $D \rightarrow A$ in Figure 1. PEEC uses the concept of partial inductances to calculate the effects on the total loop inductance as a function of frequency of all the individual conductors and current paths.

Figure 2 shows the results of the PEEC analysis from 100 Hz

to 1 MHz. It is clear that the low frequency inductance is much higher than the inductance at high frequencies. More importantly, the transition from the low frequency path begins at 1 KHz!

The low frequency inductance in Figure 2 is approximately 845 nH. This is not too far from the rough calculation of 733 nH from equation (1). So this equation is reasonable as a rough calculation for this geometry and when the conductor coupling is low.

The high frequency inductance in Figure 2 is approximately 220 nH. You will recall that the per-unit-length approach with a simple calculator resulted in a high frequency inductance of 211 nH. Again, this per-unit-length approach appears to give a good approximation to the total loop inductance at high frequencies.

The actual value of loop inductance in the transition region is very complex, and cannot be calculated without using partial inductances and numerical methods since there are multiple return current paths.



Figure 2. U-Shaped Microstrip Trace Inductance from PEEC Analysis

Return Current Path

Fullwave electromagnetic simulations using the Method of Moments can illustrate where the currents will travel on a PCB at different frequencies. Naturally, the drive currents will be constrained to travel on the trace itself (since the current is driven onto the trace), but the return current path will change as frequency increases.

Figure 3 shows the current density on the PCB at 1 KHz. The current is seen to travel along the trace, and then cut straight back to the source across the ground-reference plane.

When the frequency is shifted to 1 MHz, the currents travel a very different path. At this frequency, the return currents do not travel directly from the load to the source, but rather travel along under the trace (Figure 4). While this is a much longer path than used in Figure 3, the inductance is much lower, and therefore the impedance is lower.

Figure 5 shows the return current for 50 KHz where some of the return current takes the direct (shortest) path, and some of the return current takes the longer, lower inductance path.



Figure 3. Current Density at 1 KHz



Figure 4. Current Density at 1 MHz



Figure 5. Current Density at 50 KHz

Summary

The return current path will always find the path of least impedance. This impedance will be dominated by inductance at high frequencies. The low frequency inductance can be calculated to a first order approximation with a simple rectangular loop formula and the high frequency inductance can be found using a standard per-unit-length approach. The frequency where the inductance begins to dominate over the resistance is very low, usually in the low KHz range.

References

- EMC Video Principles Seminar, Missouri Institute of Science and Technology, http://emclab.mst.edu/inductance/rectgl.html (originally derived from Biot-Savart Law).
- [2] University of Science and Technology Electromagnetic Compatibility Laboratory Calculators. http://emclab.mst.edu/pcbtlc2/

Acknowledgement

I would like to express my gratitude to the interesting and enlightening conversations on inductance with Dr. Albert Ruehli and Professor Clayton Paul, who are well known for their expertise in this area.

Design Tid-Bit

We all know that routing a PCB trace over a split in the reference plane (for example, when the next layer has two power supply islands) is a bad idea. However, there are many cases with other considerations when this can not be avoided. Be aware that not only will local emissions increase above the board, but high speed signal energy traveling on the trace will couple below the reference plane to other traces and/or between other plane pairs.

— Bruce Archambeault