SIERRA CIRCUITS

High-Speed PCB Design Guide

Foreword

Why would we write on a topic that has been written about numerous times? What are we trying to say that is different from what has already been said? Through this design guide, we make an attempt to convey the design aspects from a manufacturing perspective and the fine details that make a big impact - not just the theoretical, but also the practical elements. We started offering design layout services because, for our customers, it comes down to completing the project on schedule and knowing that the design will work in thousands as well as in ten-piece prototypes.

The impractical design decisions made at the initial design stage will eventually get baked into the prototype, stay through the lifecycle of the product, and inadvertently cause quality defects and/or increase costs over the long term. Yes, a design review can help! But how often do you see a PCB manufacturer at the table in a design review? And it's not a one-meeting solution.

Designing an optimum PCB that is manufacturable requires immense practical experience. This practical experience is gained from processing thousands of designs and understanding the ramifications of placing a via too close to a trace, selecting a suitable component instead of an obsolete one, designing a stack-up to reduce the EMI issues from the outset and much more.

We have tried to distill the basics of what we believe every electrical engineer and designer should perceive when it comes to high-speed PCB designing. We will address most of the important design techniques and hope that we will be able to impart something that you didn't know before.

Amit Bahl
Director of Sales & Marketing at Sierra Circuits
email: amit@protoexpress.com

Table of Contents

1. Introduction to High-Speed PCB Design

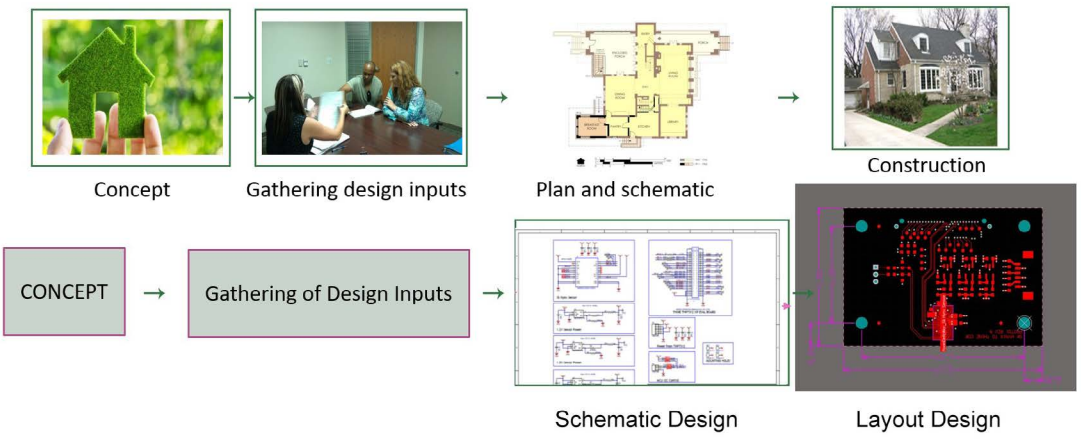
In the modern world, complexity of electronic products has increased due to the demand for higher performance such as faster data transfers, better image processing, higher computing power, and greater functionality. This has resulted in higher component count in PCBs, higher signal frequencies of the order of 5GHz and more, high-speed interfaces such as HDMI, DDR-3/4, Gigabit ethernet, and HDI (High Density Interconnect) PCB technologies having blind and buried microvias. In the future, the demand for even higher performance from computers, mobiles, and communication devices would require PCBs to be designed to cope with even higher speed of operation and higher component densities.

This booklet addresses the high-speed PCB design challenges and the best practices to be followed to meet those challenges.

It may seem obvious to state that high-speed design requires special care which is generally not needed in low speed design. High-speed designs are also usually more complex nowadays.

1.1 PCB Design Flow in General

To state very briefly, an electronic product goes through different stages from product design concept, to product requirements and specifications document (including the list of key electronic components/devices and key communication interfaces to be used), to circuit schematic design, to PCB design, and finally to the PCB manufacturing and PCB assembly.



Definition of product concept, writing the detailed product requirements, and design of the circuit schematics are mainly the responsibilities of a system designer.

During schematic entry, care needs to be taken while breaking up the design into functional blocks, bringing all related components on one page and also clearly marking the high-speed connections and power connections. For example, Ethernet related components, which run typically at 50MHz or more, are accumulated on one page of the schematic design. The differential and single ended impedance controlled lines must be clearly marked on the schematic. Also, the high current traces and voltages need to be designated. This will help the PCB designer to decide the component placement strategy and routing strategy.

As schematics are finalised, the BOM should also be validated and approved by the system designer.

Once these are done and made available to the PCB designer, then the PCB design plan needs to be worked out. As a first step, the high-speed nature and complexity of the design must be properly assessed. Based on these assessments, the appropriate PCB technology is chosen and a stackup is designed.

The PCB layout design is the next stage which includes components footprints creation, setting of the DRC parameters such as trace width, trace spacing, via padstacks, identifying controlled impedance traces and setting their rules, component placement, and routing. As the placement and the routing are done, all the best practices to reduce signal integrity problems and EMI are considered. All these concepts will be discussed in detail in subsequent sections.

Once the PCB design is complete, reviewed, and approved by all the stakeholders, it goes for PCB fabrication and ultimately PCB assembly.

It is extremely important that the PCB designers ensure that the design is manufacturable and can be successfully assembled. So, before committing to manufacturing, the designers should thoroughly review the design from a Design for Manufacturability (DFM) and Design for Assembly (DFA), perspective.

1.2 How Does One Decide if it is a High-Speed Design?

To execute a successful PCB design for a circuit board, one has to first determine if it is in fact a high-speed design. If it is a high-speed design, then the PCB designer would need to take special care during the design process; and we would call them as high-speed design considerations – the main subject of this booklet.

1. In most cases, based on their past experience, the system design engineering team may determine that this would be a high-speed design. The design team must accept this, and can verify it by means of the process described below.

2. Occasionally, it might not be explicitly stated that the design is a high-speed one; in that case the design team should determine if the design involves high-speed.

In order to decide if the PCB requires high-speed design, we follow a two step process:

Firstly, the system designers must state the values of one or more of the following parameters of design (these characterise the high-speed nature of the circuitry):

- The maximum frequency (Fm)content in the highest speed signals in the circuit.
- The fastest rise (or fall) time (Tr) of the digital signals in the circuit.
- The maximum Data Transfer Rate (DTR) applicable for signals in the circuit.

A good news is that one does not need all the above three parameters, even one will be sufficient, as it is possible to make an approximate estimate of the remaining two parameters by using the following formula:

$$F_m \approx 0.5 / T_r \approx 2.5\ DTR$$

Our objective here is to determine the highest signal frequency content i.e. F_m.

Examples:

(Ex.1) Let the fastest rise time of the digital signals be given as: Tr = 100ps (pi-co-seconds). Then, $F_m = 0.5 / (100 \times 10^{-12}\ \text{sec.}) = 5 \times 10^9\ \text{Hz} = 5\text{GHz}$.

(Ex.2) Let the highest data transfer rate be given: DTR = 5.0Gbps (Gigabits per second). Then $F_m = 2.5 \times DTR = 2.5 \times 5.0 \times 10^9\ \text{bps} = 12.5\text{GHz}$.

As a rough rule of thumb, if the highest frequency content in the signals – F_m – is greater than 50MHz, it should be treated as a high-speed design.

While the above rule of thumb is fine in most cases, there are special cases where even F_m = 60MHz may not need high-speed design considerations, and there may be some cases where even 40MHz F_m may need high speed design care.

If we want to be more certain, we carry out the following additional steps:

Secondly, we need to determine the **wavelength** (λ_m) on the PCB of the electrical (electromagnetic to be precise) signals for a given frequency, in our case Fm.

Wavelength for Fm: $\lambda_m = v / F_m$
Where: v = speed of signals on a PCB ≈ (11.8 inch/ns) I
Where: E_{reff} = Effective dielectric constant of the PCB material
Propagation Delay: $t_{pd} = 1/ v$

The speed and propagation delay for some of the commonly used PCB materials are mentioned in the following table:

Material	Er (for Stripline)	Er_{eff} (for microstrip)	V (microstrip)	V (stripline)	t_{pd} microstrip	t_{pd} stripline
Vacuum or air	1	1	11.8 in/ns	11.8 in/ns	85 ps/in	
Isola 370HR	4.0	2.92	6.90 in/ns	5.9 in/ns	145 ps/in	170 ps/in
Isola I-SPEED	3.64	2.69	7.20 in/ns	6.18 in/ns	139 ps/in	162 ps/in
Isola I-Tera MT40	3.45	2.57	7.36 in/ns	6.35 in/ns	136 ps/in	158 ps/in
Isola MT77 /Tachyon100G / Rogers 3003	3.0	2.28	7.8 in/ns	6.8 in/ns	128 ps/in	147 ps/in
Rogers 4000 series	3.55 – 3.66	2.63 – 2.7	~7.20 in/ns	~6.20 in/ns	~139 ps/in	~161 ps/in

Knowing speed 'v' from above, we can calculate the wavelength 'λ_m' for a given frequency F_m .

Now the rule of thumb: If the length of an interconnection $l < \lambda_m /12$, then we do not need to consider it as a high speed interconnection. If $l \geq \lambda_m /12$, then we do need to consider it as a high speed interconnection.

There is one caveat here: while mostly, we would be considering l here for the length of PCB interconnection, it may happen the particular interconnection goes outside the PCB through a connector to a long cable; in that case we need to consider the entire length of the interconnection.

Let us illustrate by some examples:

Assuming PCB material FR4 (370HR), we have v = 6.9 in/ns (microstrip) and 5.9 in/ns (stripline).

For F_m = 50MHz, minimum λ_m = 5.9 in/ns / 50MHz = 118 inch. Here Minimum λ_m /12 = 9.8 in. Hence, if interconnection length l < 9.8 in, (which is likely to be the case if PCB size is < 8"x 8") we may consider it as low speed, but if l ≥ 9.8 in, which maybe the case for a PCB size of ≥ even 6"x 8", we must consider it as high-speed one.

For F_m = 100MHz, minimum λ_m = 5.9 in/ns / 100MHz = 59 inch. Here Minimum λ_m /12 = 4.9 in. Hence, if interconnection length l < 4.9 in, (which is likely toi be the case if PCB size is around 2"x 3") we may consider it as low speed, but if l ≥ 4.9 in, which will be likely for a PCB size of around 4"x5" or greater, we must consider it as high-speed one.

For F_m ≥ 1GHz, minimum λ_m ≤ 5.9 in/ns / 1GHz = 5.9 inch. Here Minimum λ_m /12 ≤ 0.5 in. In any PCB, the interconnection length is likely to exceed this; Hence, we must consider it as high-speed one.

We thus see that the PCB size and therefore the interconnection lengths also play an important role in determining which interconnections are to be treated with high-speed design considerations.

1.3 Complexity of Design

In addition to high-speed design considerations, we also need to assess the complexity of the design since it also requires special design considerations.

The prime factors that play a crucial role in the design complexity are:

- Component density components count/size of board
- Routing density required
- Pitch of high pin count devices like BGAs :
  - Fine pitch BGAs (0.5mm, 0.4mm pitch) with >16 pins count. These invariably require blind and buried vias for proper IO fanouts.
  - Number of pins in a BGA exceeds 250

- Types of interfaces: HDMI, Gigabit ethernet, DDR3, etc.
- PCB technology to be used:

- Small form factor board (1”x 1”) with more than 50 components
- Larger size boards with more than 500 components
- Designs requiring impedance control 100Ω differential lines, 50Ω single-ended lines, and more than 500 components
- Any design which takes more than two weeks to layout
- The density of component pins exceeds 110 pins per square inch (17 pins per square cm)
- The density of component parts exceeds 10 parts per square inch (1.55 per square cm)
- The circuit requires mixed technology of digital, radio frequency (RF), or analog
- The board requiring mixed materials for construction
- The board has which has stringent electrical constraints
- Boards having layers 8 to 12 layers or more, depending on the complexity

1.4 High-Speed Design Considerations

There are special considerations one needs to take when designing a high-speed PCB:

1. All high-speed interconnections need to be designed as transmission lines and not just as point to point interconnections to reduce signal distortion, crosstalk and electromagnetic radiation.
2. All causes of signal degradations need to be kept under control within acceptable limits.
3. Adequate PCB technology is to be chosen so as to meet the demands of component density, wiring density, communication protocols, and complex devices.
4. All causes of unacceptable levels of electromagnetic radiation need to be kept under control.
5. Adequate power integrity has to be maintained in spite of high-frequency noise on power and ground rails in high-speed circuits – ensuring adequate power supply voltages are maintained at all the electronic devices and components for them to function properly.
6. Adequate and special PCB routing schemes need to be adopted to meet the demands of component density, wiring density, communication protocols, and complex devices.

The first three of the above points are usually covered under the disciplines called **Signal Integrity** and **PCB stackup design**, the fourth point is covered under the discipline called **EMI**,

the fifth is covered under **Power Integrity**, and the sixth under **Special layout routing techniques**.

We will now discuss these in requisite details in the following sections and chapters of this booklet.

2.Signal Integrity for PCB Designers

The moment you hear the term signal integrity, you might start yawning. But once you have an understanding of it, you will be a master in this field for sure.

Let's get straight to the point.

2.1 What is Signal Integrity?

Signal Integrity (SI) signifies the signal's ability to propagate without distortion. Signal integrity is nothing but the quality of the signal passing through a transmission line.

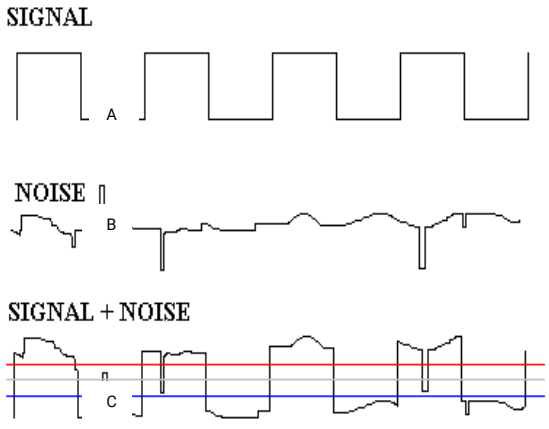
Fundamentally, signal integrity issues must be taken care of during the PCB design phase. Once the PCB has been designed, there is little one can do to improve signal integrity.

A simple analogy for your understanding:

AM signal -> not so clear (distorted signals)

FM signal -> more clear (better signal integrity)

To be more descriptive, signal integrity is the measurement of the quality of an electrical signal typically in electronic printed circuit board. In digital electronics, a stream of binary values is represented by a voltage (or current) waveform. However, digital signals are fundamentally analog in nature, and all signals are subject to effects such as noise, distortion and loss.



Over short distances and at low bit rates, a simple transmitting line can transmit with sufficient fidelity. At high bit rates and over longer distances, transmitting lines can have different effects and degrade the electrical signal to the point where errors occur and the system or device fails.

However, as speed increases, high-frequency effects take over and even the shortest lines can suffer from problems such as ringing, crosstalk, reflections, and ground bounce, seriously hampering the integrity of the signal.

Figure A above shows an ideal signal. Figure C shows the effect of noise on an ideal signal. In the following sections, we discuss the effects of a noisy signal on data integrity. In short, a noisy signal could result in bad data and therefore faulty operations.

2.2 Need for Signal Integrity

Signal integrity signifies the signal's ability to propagate without distortion.

When we have signal integrity issues in a PCB, it may not work as desired. It may work in an unreliable manner – works sometimes and sometimes not. It may work in the prototype stage, but often fail in volume production; it may work in the lab, but no reliably in the field; it worked in older production lots, but fails in new production lots, etc.

A signal is said to have lost its integrity when:

- It gets distorted, i.e. its shape changes from the desired shape
- Unwanted electrical noise gets superimposed on the signal, degrading its signal to noise (S/N) ratio
- It creates unwanted noise for other signals and circuits on the board

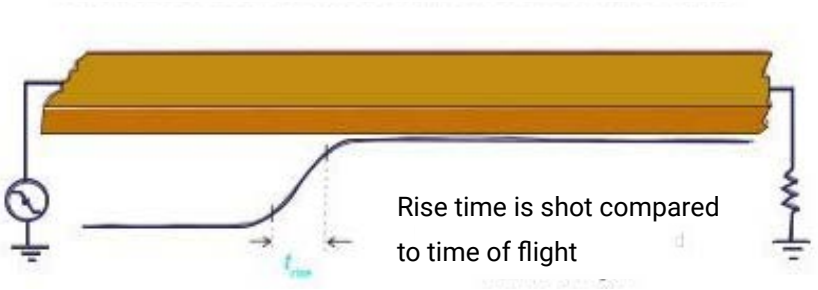
A PCB is said to have requisite signal integrity when:

- All signals within it propagate without distortion
- Its devices and interconnections are not susceptible to extraneous electrical noise and EMI – electromagnetic interference – from other electrical products in its vicinity as per or better than regulatory standards
- It does not generate or introduce or radiate EMI in other electrical circuits/cables/products either connected to it or present in its vicinity, as per or better than regulatory standards

2.3 What Leads to Signal Integrity Issues in a PCB?

Perhaps the most important cause of signal integrity issues in a PCB is faster signal rise times. When circuits and devices are operating at low-to-moderate frequencies with moderate rise and fall times, signal integrity problems due to PCB design are rarely an issue. However, when we are operating at high (RF & higher) frequencies, with much shorter signal rise times, signal integrity due to PCB design becomes a very big issue.

SIGNAL EDGE MOVING ACROSS A TRACE IN HIGH-SPEED



Factors that contribute to signal integrity degradation:

Generally speaking, fast signal rise times and high-signal frequencies increase signal integrity issues.
For analytical purposes, we can divide various signal integrity issues into the following categories:

2.3.1 Impedance discontinuities

As we mentioned earlier, if the signal encounters a discontinuity in impedance during its travel, it will suffer reflections which cause ringing and signal distortion. Discontinuities in the line's impedance will occur at the point of encountering one of the following situations:

- When a signal encounters a via in its path.
- When a signal branches out into two or more lines.
- When a signal return path plane encounters a discontinuity, like a split.
- When line stubs are connected to signal lines and are 1/4th the wavelength of the switching speed of the driver.
- When a signal line starts at the source end.
- When a signal line terminates at the receiver end.
- When signal and return paths are connected to connector pins.

And, faster the signal rise time, greater will be the signal distortion caused by impedance discontinuities.

We can minimize signal distortion due to line impedance discontinuities by:

- Minimizing the effects of discontinuities caused by vias and via stubs by using smaller microvias and HDI PCB technology.
- Reducing trace stubs lengths.
- Routing traces in daisy chain fashion rather than multi-drop branches when a signal is used at more than one place.
- Proper terminating resistors at the source.
- Using differential signaling and tightly coupled differential pairs, which are inherently more immune to discontinuities in signal return path planes.

2.3.2 Reflections, Ringing, Overshoot and Undershoot

What is Reflection?

When a signal is transmitted in a transmission line, some of the signal power may be reflected back to its transmitter rather than being carried all the way along the trace to the far end. Whenever the impedance changes in a circuit, some amount of reflection will happen. The reflected signal will travel back until it encounters another change in impedance and gets reflected again.

Influence of reflection:

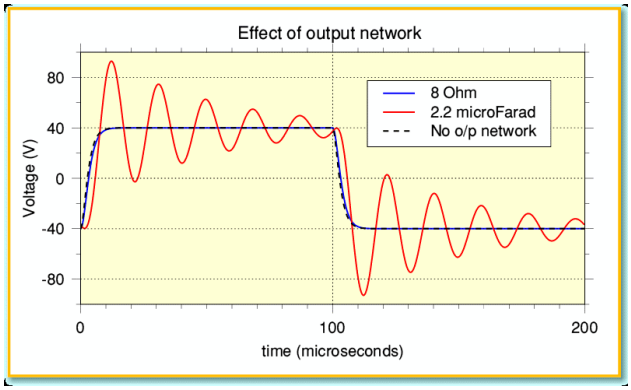
- Signal distortion caused by reflection
- Overshooting and undershooting caused by reflection

How to reduce reflection noise:

- Maintain the constant impedance
- Maintain good ground grading
- Use series termination resistor and place near the source point

What is Ringing?

Ringing is a voltage or current output that oscillates like a ripple on a pond when it's seen on an oscilloscope. The oscillation is a response to a sudden change in the input signal, like turning it on or switching.



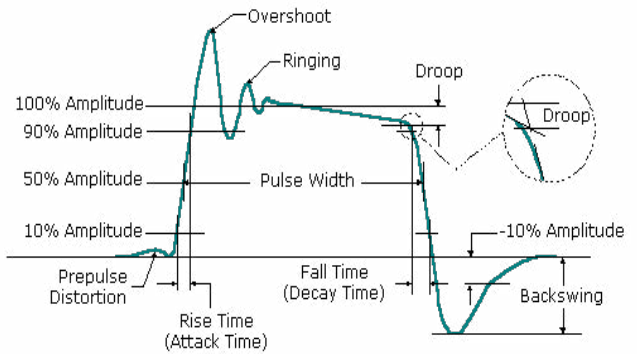
Daniel Beeker and **Rick Hartley** explained, "Ringing is the result of having the driver farther away from the receiver than 1/4th wavelength. This results in a first order reflection of more than the incident wave that returns to the driver and becomes a depletion wave at a lower voltage going back to the receiver, until all of the energy finally either goes into the receiver, is converted to heat in the conductors and dielectric or mostly radiates."

Influence of ringing:

- Increased EMI
- Increased current flow
- Decreased performance
- Audible feedback

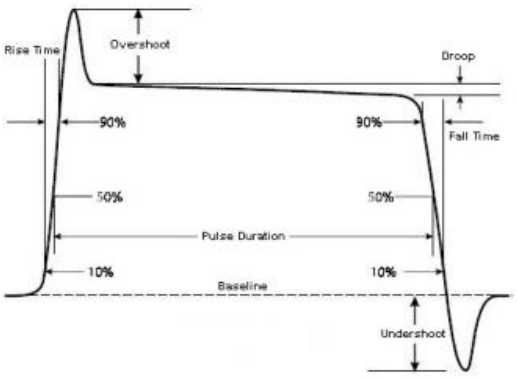
What is Overshooting and Undershooting?

A theoretical instantaneous transition of signal allowed maximum upper and lower amplitude.



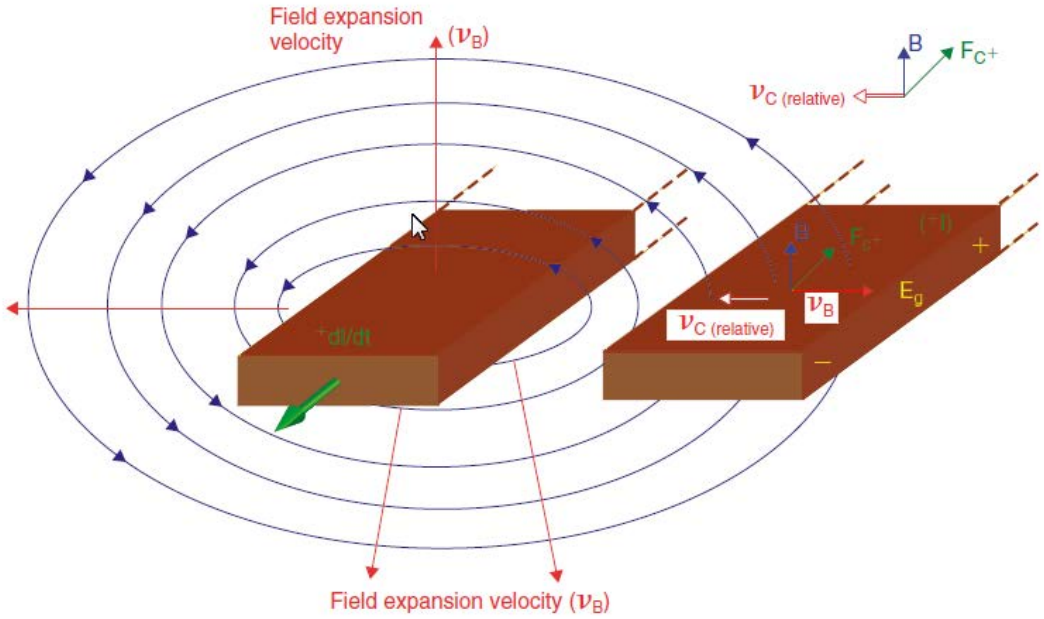
Overshoot:
When the signal transits from lower value to higher value and the value of the transit signal is more than the actual value, then overshoots occur.

Undershoot:
When the signal transits from higher value to lower value and the value of the transit signal is more than the actual value, then undershoots occur.



2.3.3 Crosstalk

One signal transmitting in one channel or circuit in a transmitting system creates an undesired effect on another circuit or channel, as shown in the below image.



Crosstalk occurs when there is coupling of energy from aggressor signal to victim signal (typically two tracks close to each other) in terms of the interference of electric and magnetic fields. The electric field is coupled via mutual capacitance between the signals. On the other hand, the magnetic field is coupled via mutual inductance between the signals.

Mutual capacitance:

When two traces run parallel to each other and are separated by a dielectric they behave as parallel plates of a capacitor and when the traces are at two different voltages an electric field is generated between them. Any variation of voltage in one of the traces will induce current in the other trace due to the electric field variation. This capacitance between two traces is called mutual capacitance.

Mutual inductance:

A trace carrying current has a magnetic field around it. If there is another trace close to the first trace carrying current this magnetic field will couple with the second trace. By Faraday's law if there is a variation in current in the first trace the magnetic field will change which will induce a voltage in the second trace. The inductance due to magnetic field coupled traces is called mutual inductance.

Techniques for decreasing crosstalk:

- Increase the spacing between signal lines as much as routing restrictions allow.The magnitude of the energy in the space is reduced by the square of the distance.
- When designing the transmission line, the conductor should be placed as close to the ground plane as possible. This couples the transmission line tightly to the ground plane and decouples it from adjacent signals.
- Implement differential routing techniques where possible.
- To avoid coupling, the signals should be routed on different layers orthogonal to each other.
- Reduce parallel run lengths between signals.

Crosstalk Noise

A fast voltage or current transition on a signal line or return path plane may couple onto adjacent signal lines causing unwanted signals called crosstalk and switching noise on the adjacent signal lines. The coupling occurs due to mutual capacitance and mutual inductance. In uniform transmission lines, a relative amount of capacitive and inductive coupling is comparable. If there are discontinuities in transmission lines, usually inductive coupling dominates, and switching noise results. And as always, faster rise time signals create more crosstalk and switching noise.

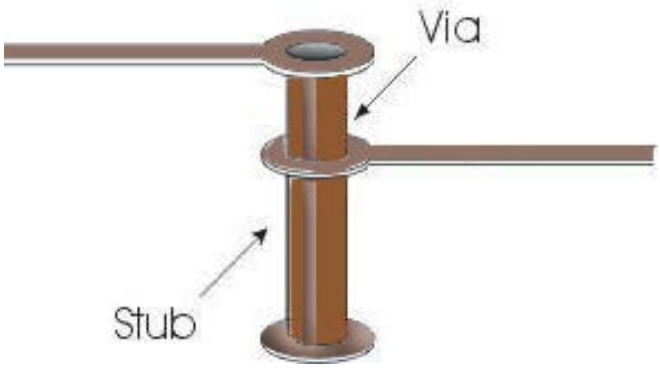
Crosstalk and switching noise can be reduced by:

- Increasing the separation between adjacent signal traces.
- Making the signal return paths as wide as possible, and uniform like uniform planes, and avoiding split return paths.
- Using a lower dielectric constant PCB material.
- Using differential signaling and tightly coupled differential pairs, which are inherently more immune to crosstalk.

2.3.4 Via Stub

When a routed signal starts from the top layer and ends with some inner layer, the remaining portion form the inner layer to the bottom layer is a via stub.

Daniel Beeker and **Rick Hartley** said, “A stub is a single piece of conductor, and unless there is a pair of vias next to each other - one ground and one signal - or a signal via and a ground plane, the field does not see the stub except as very high impedance.”



A via stub acts like a resonant circuit with a specific resonant frequency at which it stores maximum energy within it. If the signal has a significant component at or near that frequency, that component of the signal will be heavily attenuated due to the energy demands of the via stub at its resonant frequency.

2.3.5 Skew and Jitter

Signals take finite times as they travel on a PCB from source to receiver. The signal delays are proportional directly to signal line lengths and inversely proportional to signal speed on the specific PCB layers. If data signals and clock signals do not match in overall delays, they would arrive at different times for detection at the receiver, and this would cause signal skews; and excessive skew would cause signal sampling errors. As signal speeds become higher, the sampling rates are also higher, and allowable skew gets smaller, causing greater propensity for errors due to skew.

TIP:

Skew in a group of signal lines can be minimized by signal delay matching, primarily by trace length matching.

2.3.6 Signal attenuation

Signals suffer attenuation as they propagate over PCB lines due to losses caused by conducting trace resistances (which increases at higher frequencies due to skin effect) and dielectric material dissipation factor Df. Both these losses increase as frequency increases, therefore higher frequency components of signals will suffer greater attenuation than do the lower frequency components; this causes reduction in signal bandwidth, which then leads to signal distortion by increase in signal rise time; and excessive signal rise time increase results in errors in data detection.

TIP:

When signal attenuation is an important consideration, one has to choose the right type of low loss high-speed material and proper control over trace geometries to minimize signal losses.

2.3.7 Ground Bounce

Ground bounce is a form of noise that occurs during transistor switching i.e., when the PCB ground and the die package ground are at different voltages.

Techniques for decreasing ground bounce:

- Implement decoupling capacitors to local ground
- Incorporate serially-connected current-limiting resistors
- Place decoupling capacitors close to the pins
- Run proper ground

2.3.8 Power and Ground Distribution Network

Power and ground rails or paths or planes have very low, but FINITE nonzero impedances. When devices' output signals and internal gates switch states, currents through power and ground rails/paths/planes change, causing a voltage drop in power and ground paths. This will decrease the voltage across the power and ground pins of the devices. Higher the frequency of such instances, and faster the signal transition times, and higher the number of lines switching states simultaneously, greater is the voltage decrease across power and ground rails. This will reduce signals' noise margins, and if excessive, would cause devices to malfunction.

To reduce these effects, the power distribution network has to be so designed as to minimize the power system's impedance:

- Power and ground planes should be placed as close together.
- Multiple low inductance decoupling capacitors should be used across power and ground rails and they should be placed as close to device power and ground pins as possible.
- Use device packages with short leads.

2.3.9 EMI Noise

EMI increases with frequency and faster signal rise times. Radiation far-field strength increases with frequency linearly for single–ended signal currents, and squarely for differential signal currents.

3. PCB Transmission Lines and Controlled Impedance

3.1 PCB Transmission Lines

By controlling the characteristic impedance of a trace on the PCB the signal distortion can be reduced to acceptable levels. Such traces with controlled impedances of typically 50 ohms single-ended and 100 ohms differential behave as transmission lines.

A transmission line maintains the chosen impedance, Z0, from the source to the load. Additionally, they do not resonate no matter how long the trace runs, unlike other interconnections.

Transmission lines are crafted easily on PCBs by controlling materials, dimension of the traces, and by providing accurate termination resistances at source and/or load.

3.1.1 What is a PCB Transmission Line?

A PCB transmission line is a type of interconnection used for moving signals from their transmitters to their receivers on a printed circuit board. A PCB transmission line is composed of two conductors: a signal trace and a return path which is usually a ground plane. The volume between the two conductors is made up of the PCB dielectric material.

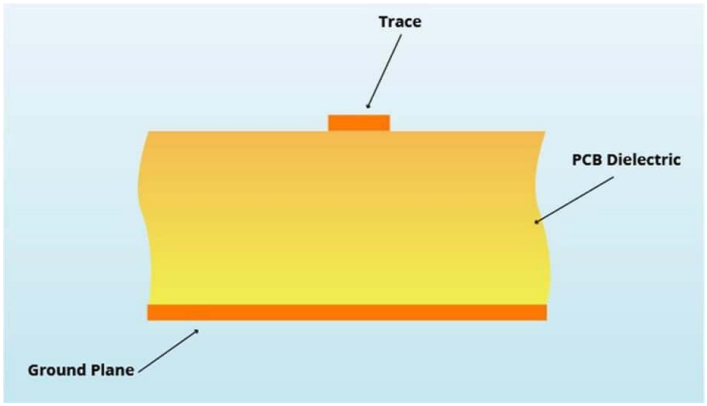
The alternating current that runs in a transmission line usually has a high enough frequency to manifest its wave propagation nature. The key aspect of the wave propagation of the electrical signals over a transmission line is that the line has an impedance at every point along its length and if the line geometry is the same along the length, the line impedance is uniform. We call such a line a controlled impedance line. Non-uniform impedance causes signal reflections and distortion. It means that at high frequencies, transmission lines need to have a controlled impedance to predict the behavior of the signals.

It is crucial to not ignore the transmission line effects in order to avoid signal reflections, crosstalk, electromagnetic noise and other issues which could severely impact the signal quality and cause errors.

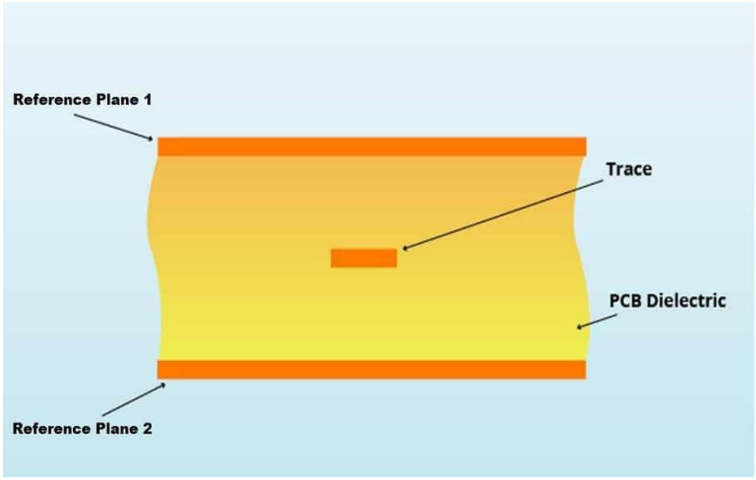
Transmission line examples:

There are usually two basic types of signal transmission line interconnects used in PCBs: microstrips and striplines. There is a third type – coplanar without a reference plane but it is not very common in use.

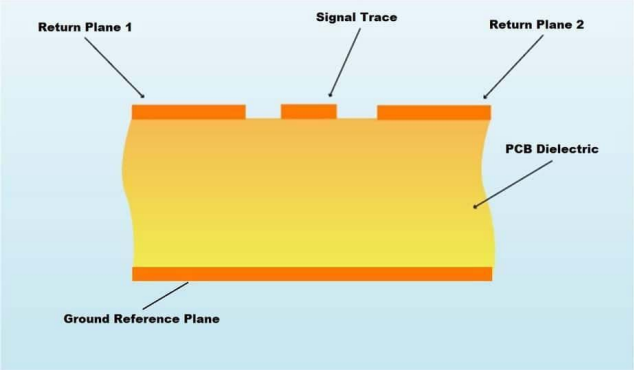
A microstrip transmission line is composed of a single uniform trace – for the signal – located on the outer layer of a PCB, and parallel to a conducting ground plane, which provides the return path for the signal. The trace and the ground plane are separated by a certain height of PCB dielectric. Below is an uncoated microstrip:



A stripline is composed of a uniform trace – for the signal – located on the inner layer of a PCB. The trace is separated on each side by a parallel PCB dielectric layer and then a conducting plane. So it has two return paths – reference plane 1 and reference plane 2.

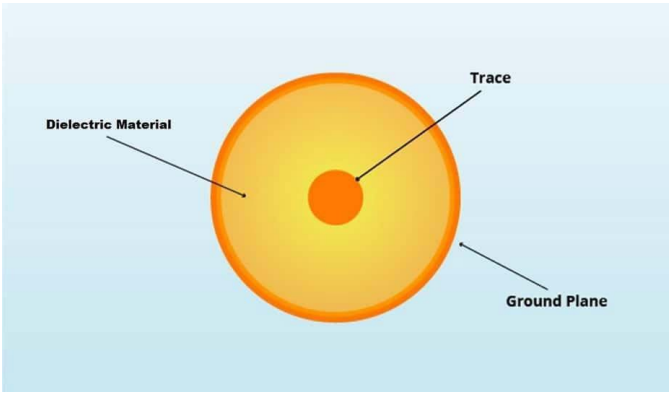


In addition to conventional microstrips and striplines described above, a coplanar waveguide structure has the signal trace and the return path conductor on the same layer of the PCB. The signal trace is at the center and is surrounded by the two adjacent outer ground planes; it is called “coplanar” because these three flat structures are on the same plane. The PCB dielectric is located underneath. Both microstrips and striplines may have a coplanar structure. Below is a coplanar microstrip waveguide with a ground plane.



Example of a coaxial cable (which is not a PCB transmission line):

A coaxial line has a circular shape and is not a PCB transmission line. This circular cable is composed of a central wire conductor for the signal and an outer circular conductor for the return path. The space between the two conductors is filled by a dielectric material. The outer conductor wire completely surrounds the signal wire. Coaxial lines are mostly used as cables for high-frequency applications, such as television, etc. A coaxial cable must have a uniform geometry of conductors and the properties of the dielectric material must be uniform along the entire geometry.



It is essential to keep in mind that a PCB transmission line is composed of not only the signal trace but also the return path, which is usually an adjoining ground plane or a coplanar conductor, or a combination of both.

3.1.2 When is an Interconnection Treated as a Transmission Line?

The set of electrical conductors (as stated above, at least two conductors are required: one for the signal and the other one for the return path, which is usually a ground plane) used for connecting a signal between its source and its destination is called a transmission line (and not just an interconnection) if it is not possible to ignore the time it takes for the signal to travel from the source to the destination, as compared to the time period of one-fourth of the wavelength of the higher frequency component in the signal.

Two very important properties of a transmission line are its characteristic impedance and its propagation delay per unit length; and if the impedance is not controlled along its entire length, or the line is not terminated by the right value of impedance, signal reflections, crosstalk, electromagnetic noise, etc. will occur, and degradation in signal quality may be severe enough to create errors in information being transmitted and received.

When the signal frequencies (in case of analog signals) or the data transfer rates (in case of digital signals) are low (less than 50 MHz or 20 Mbps), the time it will take for a signal to travel from its source to its destination on a PCB would be very small (< 10%) compared to the time period of one-fourth of a wavelength or the fastest rise time of a digital pulse signal. In this case, it is possible to approximate the interconnect by assuming that the signal at the destination follows the signal at its source at the same time. In such a low-speed scenario, the PCB signal can be analyzed by conventional network analysis techniques and we can ignore any signal propagation time or transmission line reflections, etc.

However, when dealing with signals at higher frequencies or higher data transfer rates, the signal propagation time on PCB conductors between the source and the destination cannot be ignored in comparison to the time period of one-fourth of a wavelength or the fastest pulse rise time. Therefore, it is not possible to analyze the behavior of such high-speed signals on PCB interconnects using ordinary network analysis techniques. The interconnects need to be considered as transmission lines and analyzed accordingly. The calculations for the impedances are discussed in the controlled impedance section.

3.2 The Characteristic Impedance of a Uniform Transmission Line

The relationship between V(x) and I(x) as follows:

$$Z(x) = \frac{V(x)}{I(x)} = \sqrt{\frac{R+j\omega L}{G+j\omega C}}$$

This is defined as the impedance of the transmission line at location x. Units of Z are Ohms. The parameters R, L, G and C depend on the geometry (shape, width, etc.) of the relevant PCB conductors forming the transmission line and the properties of the conductors and dielectric materials used in the PCB.

If the material and the geometrical properties are assumed to be uniform along the length of the transmission line, and the PCB materials are considered homogeneous, then R, L, G and C have the same value at every location along the length of the transmission line. This means that the above impedance has the same value for all values of x along the transmission line. This kind of transmission line is called a uniform transmission line and its impedance is:

$$Z = \sqrt{\frac{R+j\omega L}{G+j\omega C}}$$

This is the characteristic impedance of the uniform transmission line and it is its most important property from the signal integrity perspective. In the PCB industry, we generally refer to characteristic impedance as just "the impedance" of the transmission line. If the PCB manufacturing process is such that we are able to control the geometry of the PCB transmission lines within a specified tolerance range, then we could obtain the impedance value of the PCB transmission line at every location along its length within a specified tolerance of a desired value. This way, the PCB transmission line has a controlled impedance and is called a controlled impedance PCB. If we look at an infinite transmission line of characteristic impedance Z_0 from the left side at any point, we can see an impedance of Z_0 . Therefore, if we take a finite length transmission line of impedance Z_0 and terminate it on the right by an impedance of value Z_0, and if we look at the finite transmission line from the left, it will appear as an infinite transmission of impedance Z_0 from the impedance perspective:

3.3 Controlled Impedance Structures in PCBs

PCB designs are becoming smaller and faster, with each passing day. For the proper operation of circuits, the signals between components have to be noise-free and without distortion. This can be achieved by controlling the impedance of the traces.

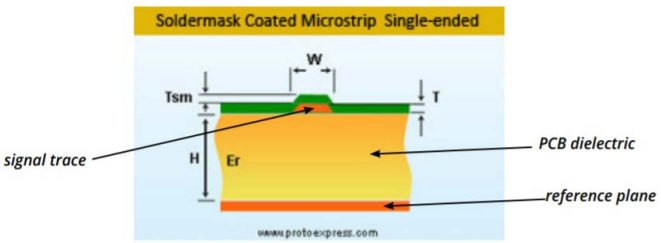
What is Controlled Impedance?

Controlled impedance is the characteristic impedance of a transmission line constituted by PCB conductors. It is relevant when high-frequency signals propagate through PCB transmission lines. Controlling impedance of a PCB trace is required to propagate signals without distortion.
The impedance of a particular circuit is determined by the physical dimensions and materials of that circuit.

Here are some of the most widely used PCB transmission lines which require controlled impedance:

3.3.1 Single-Ended Microstrip

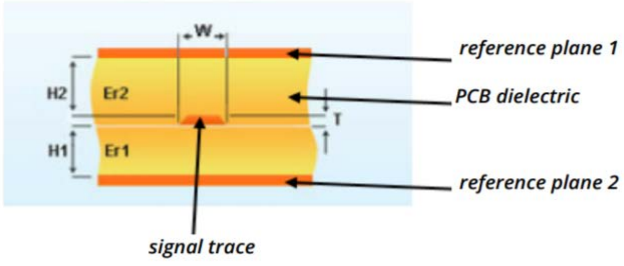
A single-ended microstrip is a transmission line composed of a single uniform conductor placed on the outer layer of a PCB. The return path for signals traveling on this line is usually provided by a conducting plane separated from the transmission line by a certain height of the PCB dielectric.



H = Height of the dielectric between the trace and plane, specified in mils
W = Width of the copper trace, specified in mils
T = Thickness of the copper trace, specified in mils
Er = Dielectric constant of the dielectric between the trace and plane

3.3.2 Single-Ended Stripline

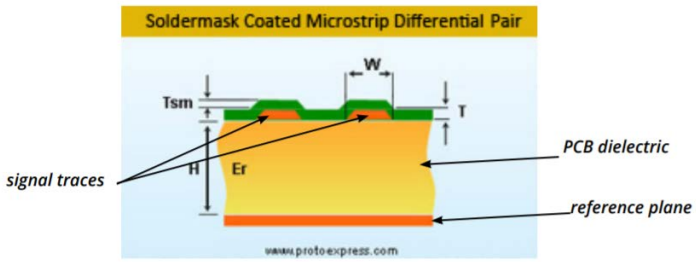
A single-ended stripline is composed of a uniform conductor on an inner layer of a PCB. It is separated on each side by a dielectric layer followed by copper planes.



H = Height of the dielectric between the trace and plane, specified in mils
W = Width of the copper trace, specified in mils
T = Thickness of the copper trace, specified in mils
Er = Dielectric constant of the dielectric between the trace and plane

3.3.3 Microstrips Differential Pair

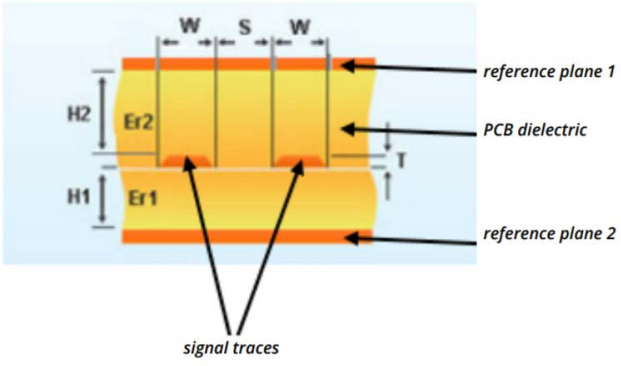
A microstrip differential pair is similar to the single-ended microstrip described earlier, except that it has a pair of conductors separated by a uniform distance between them.



H = Height of the dielectric between the trace and plane, specified in mils
W = Width of the copper trace, specified in mils
T = Thickness of the copper trace, specified in mils
Er = Dielectric constant of the dielectric between the trace and plane
S = The separation between the two traces of the differential pair

3.3.4 Striplines Differential Pair

A stripline differential pair is similar to the single-ended stripline except that it has a pair of conductors separated by a uniform distance between them.



H = Height of the dielectric between the trace and plane, specified in mils
W = Width of the copper trace, specified in mils
T = Thickness of the copper trace, specified in mils
Er = Dielectric constant of the dielectric between the trace and plane
S = The separation between the two traces of the differential pair

3.4 How to Control the Impedance?

The factors that influence impedance are the PCB materials dielectric, the trace thickness, width and height from the ground plane.

The designer should make sure that the manufacturer has the ability to provide the right pattern size, position, and tolerance. The board might turn out to be useless if these parameters aren't achieved.

The two types of commonly implemented impedance controls are:

Controlled dielectric thickness:

The designer provides the controlled dielectric stack-up to the manufacturer. Since impedance traces are not specified here, the manufacturing focus is completely upon building a board within +/- 10% tolerance of the specified dielectric thickness from layer to layer.

Impedance control:

Here the impedance is controlled through the dielectric thickness, the trace width, and space. The manufacturer performs a test to ensure that the desired impedance can be achieved using TDR coupons. Some adjustments are made depending upon results from the first articles in order to meet the designer's needs and the boards are manufactured within the specified tolerance.

A typical tolerance on the final impedance is +/- 10%. But Sierra Circuits is capable of achieving +/- 5% impedance tolerance.
A typical tolerance on the final impedance is +/- 10%. But Sierra Circuits is capable of achieving +/- 5% impedance tolerance.

3.5 Design and Manufacture of Controlled Impedance Lines

3.5.1 Determining Which Signals Require Controlled Impedance

When designing a board, designers should stick to strict guidelines for controlled impedance. They should study the datasheets of the integrated circuits to determine the specific signals that require controlled impedance. The components' datasheets provide precise instructions for impedance values for each group of signals. Usually, the data sheets mention the spacing rules and the right layers on which specific signals are to be routed.

3.5.1.1 Communication Protocols Requiring Controlled Impedance Lines

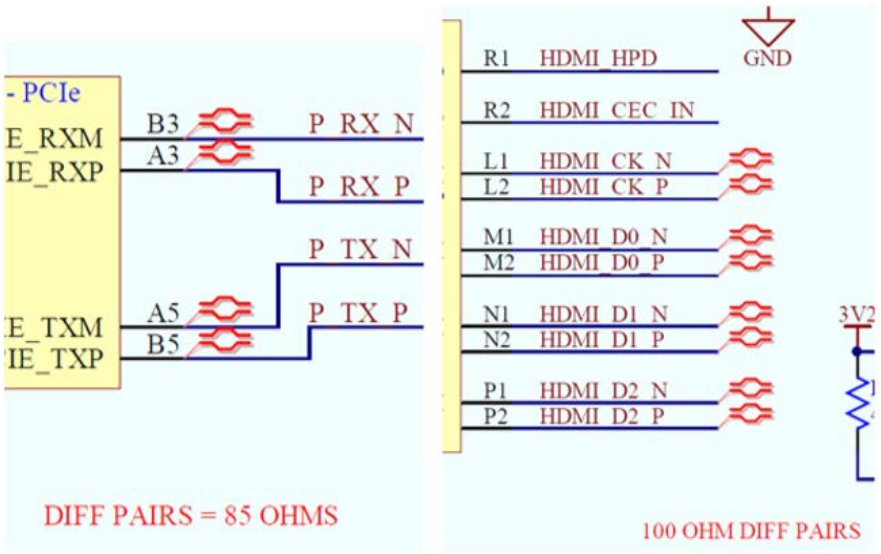
	Type of Interface	Differential Impedance	Single Ended Impedance
1	PCI Express	90Ω ±15%	50Ω ±15%
2	SATA	90Ω ±15%	55Ω ±15%
3	Ethernet	95Ω ±15%	55Ω ±15%
4	USB 2.0 Signals	90Ω ±15%	50Ω ±15%
5	USB 3.0 Signals	90Ω ±15%	50Ω ±15%
6	Parallel RGB LCN	N/A	50Ω ±15%
7	LVDS LCD	100Ω ±15%	55Ω ±15%
8	HDMI/DVI	90Ω ±15%	50Ω ±15%
9	Analogue VGA	N/A	50Ω ±15% section B 75Ω ±15% section C See Figure Below
10	Parallel Camera Interface	N/A	50Ω ±15%
11	SD/MMC/SDIO	N/A	50Ω ±15%
12	I2C	N/A	50Ω ±15%
13	Display Serial Interface (MIPI/DSI with D-PHY)	90Ω ±15%	50Ω ±15%
14	Camera Serial Interface (MIPI/CSI-2 with D-PHY)	90Ω ±15%	50Ω ±15%

3.5.1.2 Annotate the Schematic with Impedance Requirements

In the circuit schematics, the engineer should specify the controlled impedance signals and the nets should be classified as differential pairs (100Ω, 90Ω or 85Ω) or single-ended nets (40Ω, 50Ω, 55Ω, 60Ω or 75Ω). To make things clearer, the designer can append N or P after the net names for differential pair signals in a schematic.

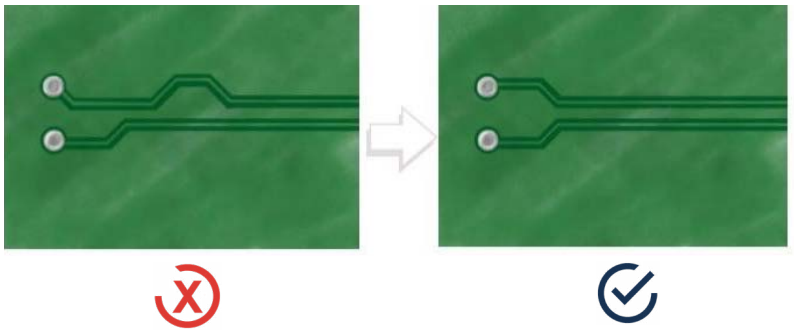
Also, the special controlled impedance layout guidelines must be specified (if any) in the schematic or in a dedicated ”Read me” file.

In the below Altium schematic, the differential pairs have appropriate net names.



3.5.2 Routing Differential Pairs

The high-speed differential pair signal traces should be routed parallel to each other with a consistent spacing between them. Specific trace width and spacing are needed to calculate the specific differential impedance. The differential pairs should be routed symmetrically. The designer should minimize areas where the specified spacing is enlarged due to pads or the ends. When differential pairs change layers and therefore change reference ground planes, ground transition vias are required which connect the two different ground references.

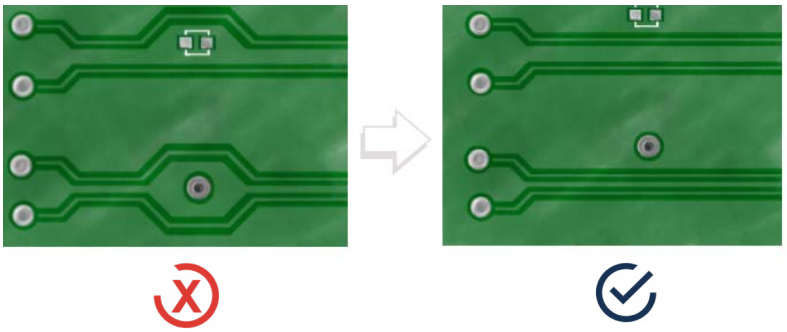


TIP:

Route differential pairs symmetrically and always keep signals parallel

3.5.3 Placing Components, Vias, and Coupling Capacitors

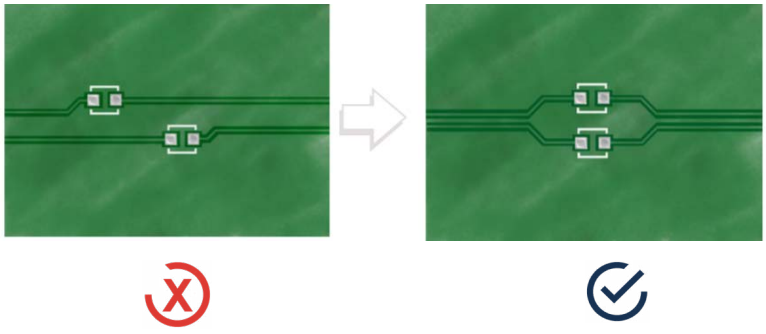
The components or vias should not be placed between differential pairs even if the signals are routed symmetrically around them. Components and vias between the differential pair signals create discontinuity in impedance and could lead to signal integrity problems. For high-speed signals, the spacing between one differential pair and an adjacent differential pair should not be less than five times the width of the trace. The designer should also maintain a keep-out of 30 mils to any other signals. For clocks or periodic signals, the keep-out should be increased to 50 mils to ensure proper isolation.



TIP:

Do not place any components or vias between differential pairs.

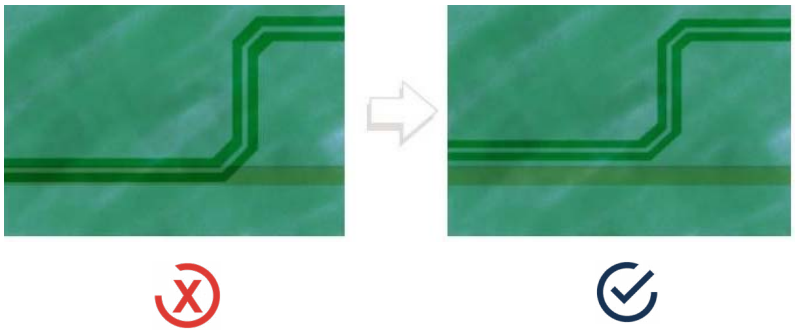
If high-speed differential pairs require serial coupling capacitors, they need to be placed symmetrically. The capacitors create impedance discontinuities, so placing them symmetrically will reduce the amount of discontinuity in the signal.



TIP:

Place coupling capacitors symmetrical.

The designer should minimize the use of vias for differential pairs, and if placed, they need to be symmetrical to minimize discontinuity.



TIP:

Do not route high-speed signals at plane and PCB borders.

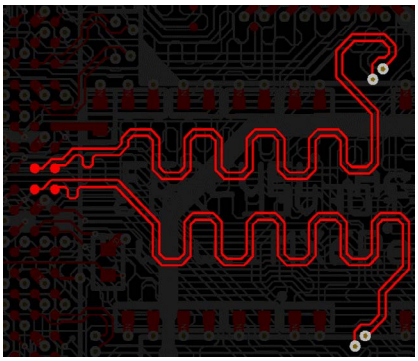
3.5.4 Length Matching

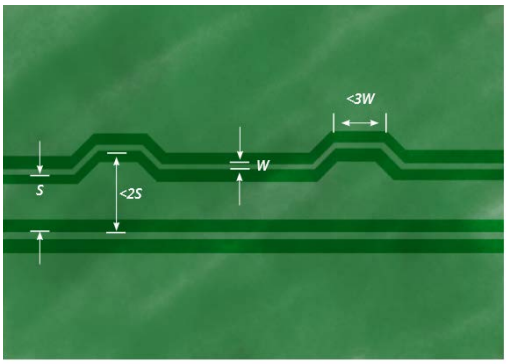
Propagation delay of a signal in a circuit is important and it should be within the specs of the components. Propagation delay depends on the physical characteristics of the trace if width, thickness, and height of the trace are the same throughout the trace then propagation delay is directly proportional to the length of the trace. Thus, in a differential pair if the delays have to be the same then their lengths should be same/matched as well.

Length matching will achieve propagation delay matching if the speed of the signals on various traces is the same. Length matching may be required when a group of high-speed signals travel together and are expected to reach their destination at the same time (within a specified mismatch tolerance). Note that, it's a good practice to **keep all the high-speed signals of the same group of signals on the same layer to avoid skew in propagation delay.**

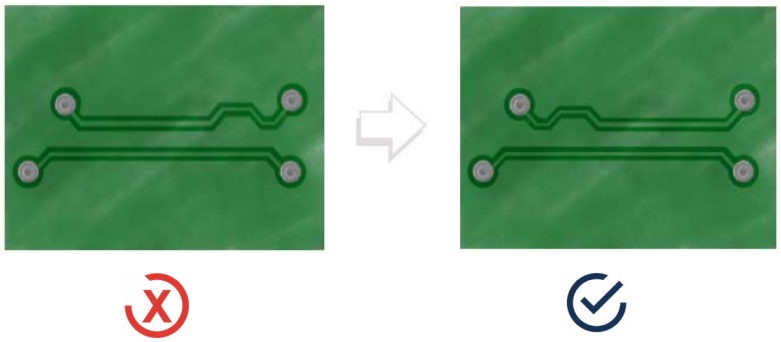
The lengths of the traces forming a differential pair need to be matched very closely, otherwise that would lead to an unacceptable delay skew (mismatch between the positive and negative signals) and the propagation delay for the traces should be within the requirements of the design. The mismatch in length needs to be compensated by using serpentines in the shorter trace. The geometry of serpentine traces needs to be carefully chosen to reduce impedance discontinuity. The figure below shows the requirements for ideal serpentine traces.

It is important to match the etch lengths of the differential pairs and add serpentine routing as close as possible to the mismatched ends. In the image below, the serpentine is added near the pads on the left side as they are farther apart from each other and hence mismatched.



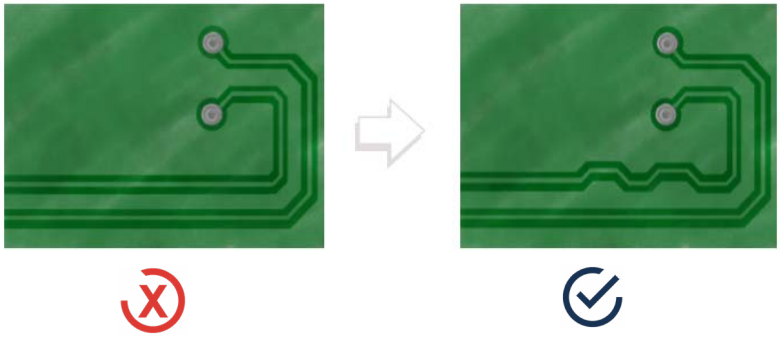


The serpentine traces should be placed as near as possible to the source of the mismatch. This ensures that the mismatch is corrected immediately. In the figure below, the mismatch occurs on the left set of vias, so the serpentine needs to be added on the left rather than the right. Similarly, bends cause mismatches making the trace on the inner bend smaller than the outer trace. Therefore, we need to add serpentines as close to the bend area. If a pair has two bends closer than 15mm, they compensate each other, hence, the addition of serpentines isn't required.



TIP:

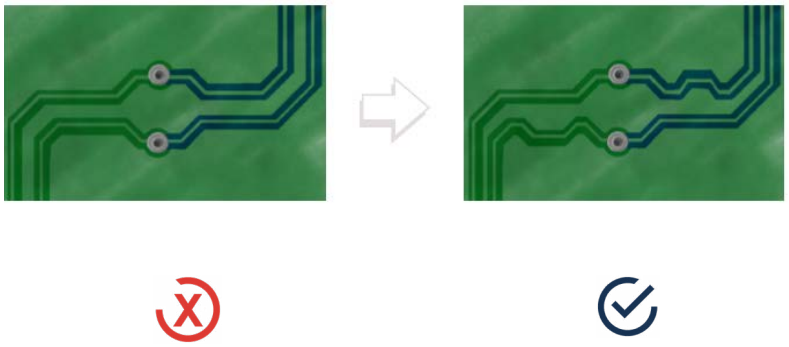
Add length correction to the mismatching point.



TIP:

Place length compensation close to bend.

When a differential pair signal changes from one layer to another using vias and has a bend, each segment of the pair needs to be matched individually. Serpentines should be placed on the shorter traces near the bend. The designer has to manually inspect for this kind of violation as it will not be caught in design rule checks (DRC) since the lengths of the total signals will be closely matched. Since the signal speed of traces on various layers may be different, it is recommended to route differential pair signals on the same layer if they require length matching.



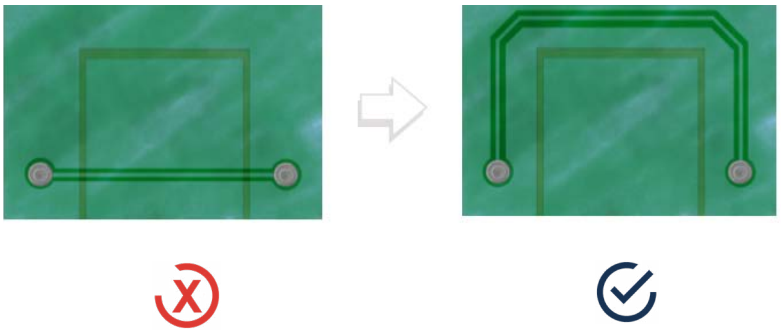
TIP:

Length differences need to be compensated in each segment.

3.5.5 Reference Layers for Return Path of Controlled Impedance Signals

All high-speed signals require a continuous reference plane for a return path of the signal. An incorrect signal return path is one of the most common sources for noise coupling and EMI issues. The return current for high-speed signals try to follow the signal path closely whereas the return current for low-speed signals take the shortest path available. Generally, the return path for high-speed signals is provided in the reference planes nearest to the signal layer.

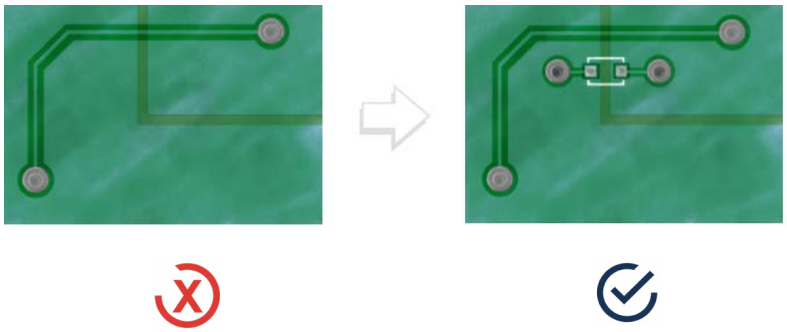
High-speed signals should not be routed over a split plane because the return path will not be able to follow the trace. The designer should route the trace around the split plane for better signal integrity. Also, the ground plane must be minimum three times the trace width (3W rule) on each side.



TIP:

Avoid routing over split planes.

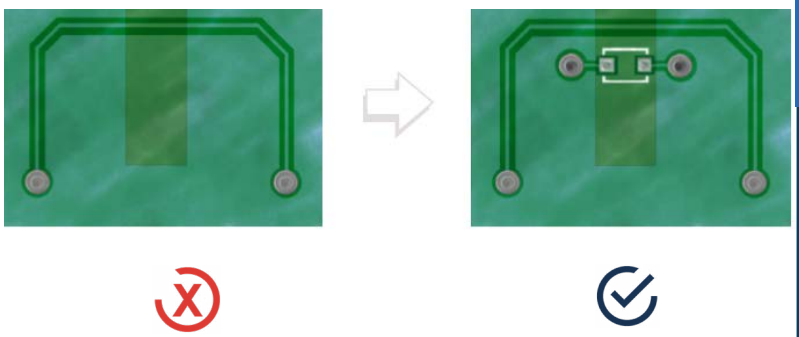
If there is absolutely no other option and a signal needs to be routed over two different reference planes, a stitching capacitor between the two reference planes is required. The capacitor needs to be connected to the two reference planes and should be placed close to the signal path to keep the distance between the signal and the return path small. The capacitor allows the return current to travel from one reference plane to the other and minimizes impedance discontinuity. A good value for the stitching capacitor is between 10nF and 100nF.



TIP:

Stitching capacitor is needed when routed over split planes. If both the references are ground then a trace bridge between the two grounds placed below the signal is a better option than a capacitor

The PCB designer should avoid both split plane obstructions and slots in the reference plane just underneath the signal trace. If the slots are unavoidable, stitching vias should be utilized to minimize the issues created by the separated return path. Both pins of the capacitor should be connected to the ground layer and should be placed close to the signal.

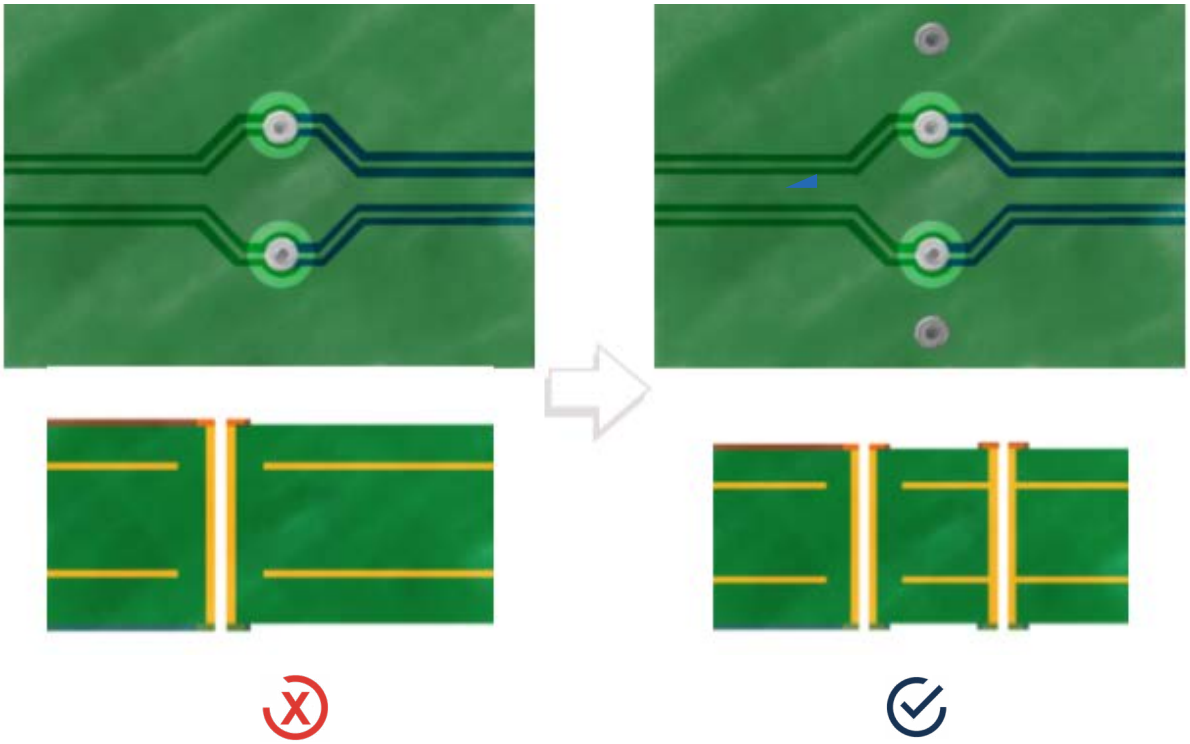


TIP:

Stitching capacitor needed when routing over plane obstructs.

When vias are placed together, they create voids in reference planes. To minimize these large voids, the designer should stagger the vias to allow sufficient feed of the plane between vias. Staggering the vias allows the signal to have a continuous return path.

If a high-speed differential pair or single-ended signal switches the layers, the designer should add stitching vias close to the layer change vias. This also allows the return current to change ground planes.



TIP:

Place stitching vias when signal changes ground reference. Preferably put the ground via between the signal vias.

3.5.6 Errors to Avoid When Designing for Controlled Impedance

3.5.6.1 Distinguishing Controlled Impedance Traces from Other Traces

The trace widths of controlled impedance traces must be distinct from the remaining traces. This makes it easy for the manufacturer to identify them.

For example, if a 5-mil trace is required to achieve 50Ω impedance and if the board has other traces routed with 5-mil widths, then the manufacturer will have a hard time identifying the controlled impedance traces. Hence, it's recommended to route the 50Ω impedance traces to 5.1-mil or 4.9-mil wide.

The table below shows an example of a design with the trace widths and spacings for controlled impedance on different layers. The non-impedance signal traces should not be routed with 3.5, 3.6, 4.2, 4.25, and 4.3-mil trace widths for this particular design.

Layer	50 Ohm	90 Ohm Trace	90 Ohm Space	100 Ohm Trace	100 Ohm Space
1	4.3 mils	4.25 mils	6.25 mils	3.5 mils	7 mils
3	4.2 mils	4.4 mils	6.1 mils	3.6 mils	6.9 mils
6	4.2 mils	4.4 mils	6.1 mils	3.6 mils	6.9 mils
8	4.3 mils	4.25 mils	6.25 mils	3.5 mils	7 mils

3.5.6.2 Traces Overpassing Split Planes

The high-speed signals must be routed over a solid ground reference plane. The traces should not be routed over a split plane or a void in the reference plane. Routing high-speed signals across split planes can produce the following issues:

- Interference with neighboring signals
- Degradation of the electrical signal thus ruining signal integrity

The designer can use stitching capacitors across split planes if the signals have to be routed over them. The capacitors contribute a return path for the high-frequency current and minimize the current loop area along with any impedance discontinuity created by traversing the split plane. In the image shown below, the signals are routed around the void in the plane rather than across the split/void.

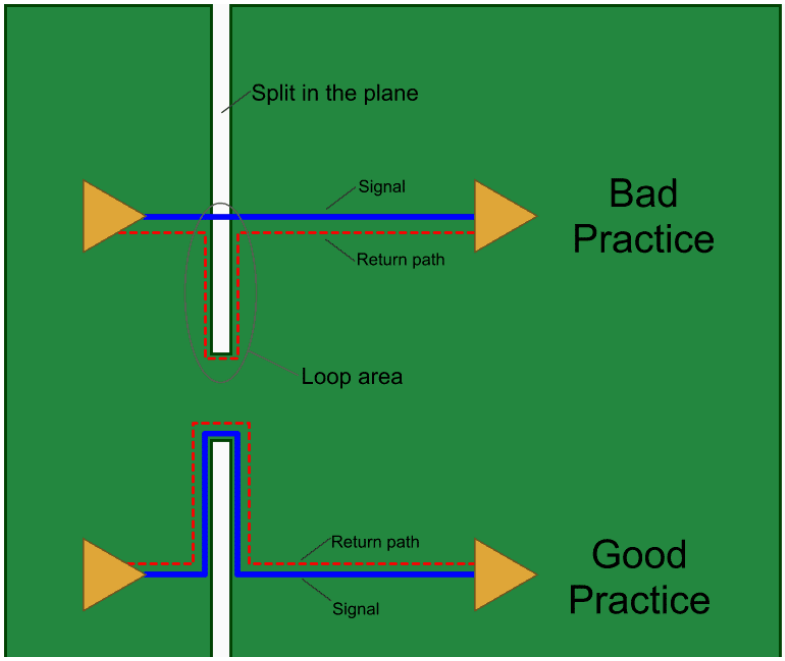


Image credit: Altium Designer

3.5.6.3 Traces with no Reference Ground Plane

The designer should route the high-speed signals either on the top or bottom layer. Also, a complete ground reference plane on the adjacent layers must be provided. The impedance will be quite high if there are no adjacent layers. The inner layers can be used for power planes and other signal routing purposes.

3.5.7 Controlled Impedance Design Checklist

- The controlled impedance lines should be marked in the PCB schematic drawing.
- The differential pair trace lengths should be matched with a tolerance of 20% of the signal rise/fall time.
- High-data frequency connectors should be used.
- For stripline construction, use ground or unbroken power, over, beneath and sides of the differential pairs. The ground and power planes provide the return currents path. This also reduces **EMI issues.**

3.5.8 Common Mistakes to Avoid in a Stack-Up for Controlled Impedance

Prepregs:

Generally, it is recommended not to use more than three different types of prepregs in a stack-up. The dielectric thickness of each prepreg layer should be less than 10 mils, otherwise, it increases the chance of a greater variation in the final thickness. Prepregs with very low-resin and high-glass content should be avoided. The low-resin content may lead to resin starvation during lamination. For example, 7628 and 2116 prepregs have low-resin and high-glass content.

Impedance trace/space:

The spacing between two traces in a differential pair should not be more than twice the width of the traces. For example, a 4-mil differential trace should not have more than an 8-mil space. Also, the trace width should not exceed twice the dielectric thickness between the target signal layer and the nearest reference layer.

3.5.9 Manufacturing Tolerances, Measurements, and Coupons

3.5.9.1 How Sierra Circuits Deals with Controlled Impedance

Equipment used by Sierra Circuits for impedance measurement:

- Polar CITS – coupons only
- Tektronix 8300 – boards as well as coupons

If an impedance test coupon is not functional or fails the impedance test, Sierra Circuits performs impedance testing on boards to verify if the product is within the specifications. It is essential to test the impedance from the boards due to the length of the traces, which depends upon the size of the board. The position of the inner layer impedance traces in the finished product is very critical as well.

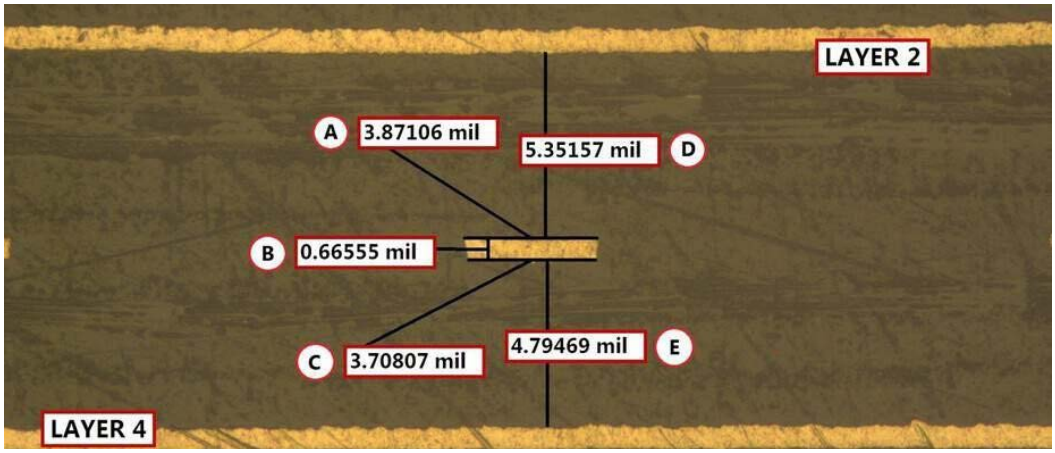
3.5.9.2 Impedance Failure Analysis During Manufacturing

Upon failure, a cross-section of the impedance coupon is taken to investigate the deviation from the calculated impedance to the recorded impedance.

The manufacturer's cross-section technician measures the dielectric thicknesses depending upon the trace location, either the inner layer or the outer layer. Additionally, the trace width is estimated from the bottom as well as the top of the affected impedance trace along with the copper thickness or the trace height.

When it is a differential pair, the spacing between the two traces is measured to understand whether or not the projected impedance is in alignment with the recorded impedance. The image shown below depicts the cross-section evaluation details on a single-ended impedance trace.

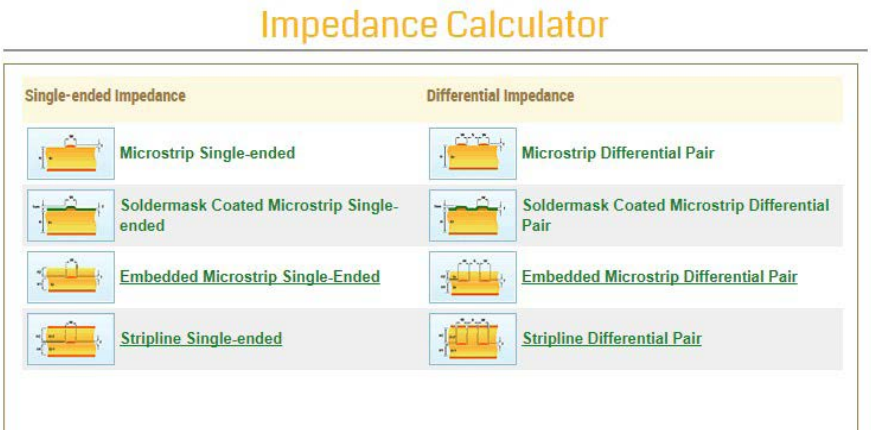
A – Trace Width from Top
B – Copper Thickness or Trace Height
C – Trace Width from Bottom
D – Dielectric Thickness between Layer 2 and Layer 3 (Trace)
E – Dielectric Thickness between Layer 3 (Trace) and Layer 4



To determine the acceptability of the boards, Sierra Circuits implements test coupons to ensure there are no variations in the trace width or the trace thickness.

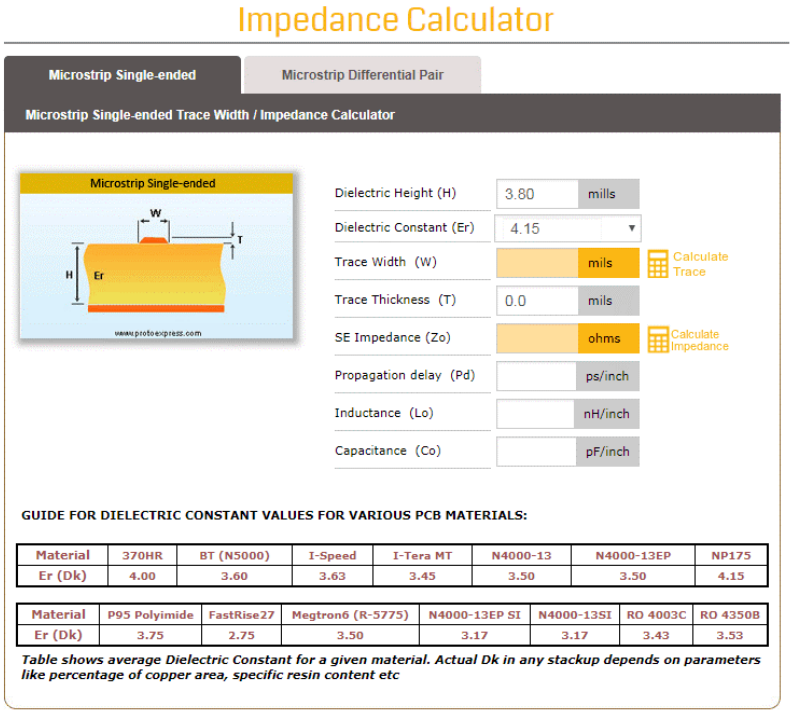
3.5.9.3 The Sierra Circuits Impedance Calculator

Designers can choose the type of impedance required: single-ended or differential.



Calculating single-ended impedance:

Next, the dielectric constant is chosen based on the materials listed in the box below. Depending on the stack-up the dielectric height is chosen. The required single-ended impedance, the trace width, and the trace thickness are entered (if not already pre-filled). Finally, the impedance is calculated once the "Calculate Impedance" or "Calculate Trace" buttons are clicked. If a specific trace width is required, the dielectric height and the trace thickness should be adjusted until desired trace width is achieved. Note: The impedance should not vary too much when the above values are changed.



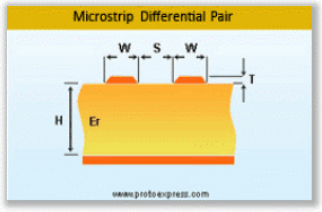
Calculating differential impedance:

In the differential impedance calculator the trace width, the dielectric height, the dielectric constant, and the trace thickness are entered. Finally, “Calculate Trace” button is clicked to obtain the accurate trace width. If a specific trace width is required, then the adjustments can be made until the desired value is obtained. Note that the impedance tolerance +/- 2%.

Impedance Calculator

Microstrip Single-ended | Microstrip Differential Pair

Microstrip Differential Pair Trace Width / Impedance Calculater



Dielectric Height (H)	3.5	mils
Dielectric Constant (Er)	4.15	
Trace Width (W)		mils — Calculate Trace
Traces Separation (S)	6.0	mils
Trace Thickness (T)	1.40	mils
Differential Impedance (Zd)		ohms — Calculate Impedance
Odd Mode Impedance	0.00	ohm
Even Mode Impedance	0.00	ohm
Common Mode Impedance	0.00	ohm
Propagation Delay	0.00	ps/inch
Inductance(Lo)	0.00	nH/inch
Capacitance	0.00	pF/inch

GUIDE FOR DIELECTRIC CONSTANT VALUES FOR VARIOUS PCB MATERIALS:

Material	370HR	BT (N5000)	I-Speed	I-Tera MT	N4000-13	N4000-13EP	NP175
Er (Dk)	4.00	3.60	3.63	3.45	3.50	3.50	4.15

Material	P95 Polyimide	FastRise27	Megtron6 (R-5775)	N4000-13EP SI	N4000-13SI	RO 4003C	RO 4350B
Er (Dk)	3.75	2.75	3.50	3.17	3.17	3.43	3.53

Table shows average Dielectric Constant for a given material. Actual Dk in any stackup depends on parameters like percentage of copper area, specific resin content etc

Disclaimer:

In both cases, Sierra Circuits’ stack-up team does not check the odd mode impedance, the even mode impedance, the propagation delay, the inductance, or the capacitance. The reason is that most boards only require one or two types of impedance: single-ended and differential.

4. PCB Stackup Design & PCB Technology

4.1 PCB Stackup Design

High-speed designs demand critical signal integrity requirements and crafting a PCB with the right stack-up becomes part of the overall signal integrity equation. The selection of the PCB materials for impedance, dissipation, and other signal characteristics along with the right order and number of layers of the materials, need to be considered.

A stack-up, also known as build-up, is the construction of a multilayer PCB in a sequential order. Almost 99% of the time, the stack-ups will be symmetrical. The stack-ups are made up of cores, prepregs and copper foils. The majority of the products fall under 62-mil board thickness.

4.1.1 Construction of a Stackup

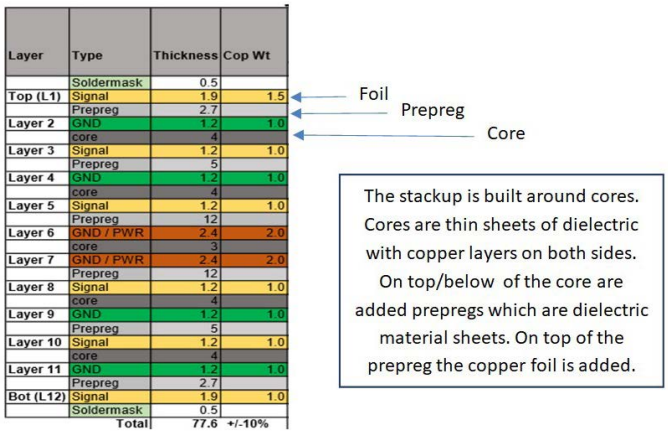
Depending on the construction type, stackups are classified into:

- Core construction (99% results, employed for military and aerospace)
- Foil construction (97% results)

The different types of stack-ups are:

- Standard
- Hybrid – involves two different types of dielectric material for different layers
- HDI

A PCB stackup of layers consists of various layers which include cores, prepregs and foils.



Layer	Type	Thickness	Cop Wt
	Soldermask	0.5	
Top (L1)	Signal	1.9	1.5
	Prepreg	2.7	
Layer 2	GND	1.2	1.0
	core	4	
Layer 3	Signal	1.2	1.0
	Prepreg	5	
Layer 4	GND	1.2	1.0
	core	4	
Layer 5	Signal	1.2	1.0
	Prepreg	12	
Layer 6	GND / PWR	2.4	2.0
	core	3	
Layer 7	GND / PWR	2.4	2.0
	Prepreg	12	
Layer 8	Signal	1.2	1.0
	core	4	
Layer 9	GND	1.2	1.0
	Prepreg	5	
Layer 10	Signal	1.2	1.0
	core	4	
Layer 11	GND	1.2	1.0
	Prepreg	2.7	
Bot (L12)	Signal	1.9	1.0
	Soldermask	0.5	
	Total	77.6	+/-10%

The stackup is built around cores. Cores are thin sheets of dielectric with copper layers on both sides. On top/below of the core are added prepregs which are dielectric material sheets. On top of the prepreg the copper foil is added.

4.1.2 Stackup Design

The PCB construction depends on the component packages used in the design, required signal trace density, and impedance matching requirements. For the high-speed PCBs, using a multilayer PCB with buried ground and power supply planes is mandatory. Solid copper planes allow designers to keep the device ground and power connections short. Further, the ground plane offers low inductance return paths for the high-speed signals.

We hear from our PCB manufacturing team that there are cases where designers spent hundreds of labor hours on designing PCBs which ultimately had to be trashed. This is because the designers failed to understand the manufacturability of these complex designs.

Just so that this doesn't happen to you, have a look at the below mentioned pointers.

Tips for an optimum design:

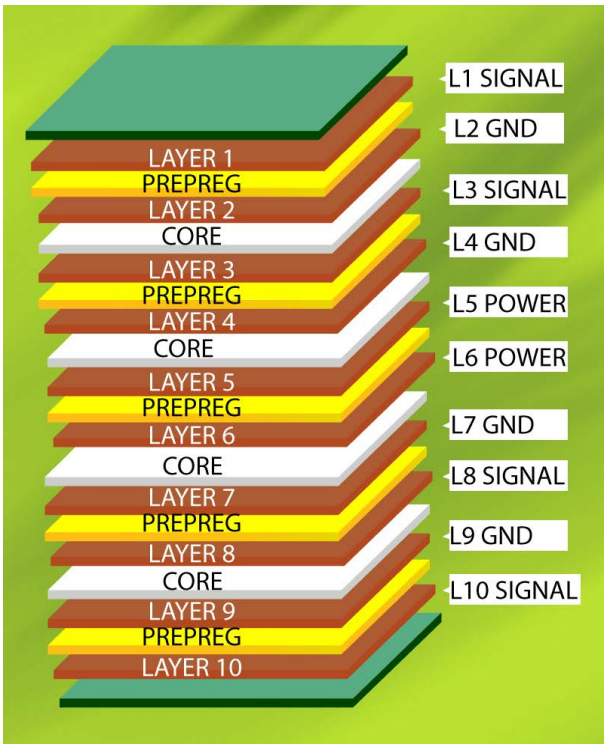
- Maintain minimum aspect ratio:
  - o 1:10 for through-hole
  - o 1:0.75 for microvias
- Implement microvias to bring down the board thickness.
- In sequential lamination, do not exceed more than 3 lamination cycles. More than 5 or 6 laminations might create problems.
- When there are numerous connections through blind vias, always incorporate a back drilling option to minimize the lamination, drill and fill cycles.
- When the line widths are 3 mils, the start copper should be 9 microns.

4.1.3 Best Way to Do a Stackup for High-Speed Signals

The complex components on the board, like the BGAs, determine the PCB stack-up. The complexity of the BGA and the pitch of the BGA, either 0.8, 0.5 or 0.4, would determine the stackup design. For fine pitch BGA of 0.5mm and less, it's recommended to have a stackup of at least 10 layers with buried vias and via-in-pads. For instance, if a 9 X 9 or a 10 X 10 BGA is used, then the designer needs to fan out the nets in the right manner. Likewise, if a 0.5mm BGA is incorporated, then through-hole vias can be used to fan it out assuming it's not too populated. But if a 0.4mm BGA is considered, then blind and buried vias are implemented for routing purposes. As a result, it adds up more layers in the stackup.

The PCB designer should figure out the number of layers required to fan out a BGA. Consequently, the designer determines on which layers the critical signals are routed and the number of power and ground layers required. All these parameters will determine the number of layers in the stackup.

This is what a preliminary stackup looks like:



10-layer stackup with signal layers

12 Layer	Drills & µVias	Foil / Core / Prepreg Details	CU Oz / Th. Mils	Dk @ 10GHz	Plating Mils	12 L Cl-1	Cu %	Final Thickness
		Solder mask	0.500	4.20				0.500
12L-1		CU Foil	0.25		1.1	S	100%	1.450
		3.6 Mil Prepreg	3.600	3.63				3.348
12L-2		Copper	0.5		0	P	64%	0.700
		4 Mil Core 0.5/0.5	4.000	3.84				4.000
12L-3		Copper	0.5		0	S	24%	0.700
		7.2 Mil Prepreg	7.200	3.63				6.416
12L-4		Copper	0.5		0	P	64%	0.700
		4 Mil Core 0.5/0.5	4.000	3.84				4.000
12L-5		Copper	0.5		0	S	24%	0.700
		7.2 Mil Prepreg	7.200	3.63				6.416
12L-6		Copper	0.5		0	P	64%	0.700
		4 Mil Core 0.5/0.5	4.000	3.84				4.000
12L-7		Copper	0.5		0	P	64%	0.700
		7.2 Mil Prepreg	7.200	3.63				6.416
12L-8		Copper	0.5		0	S	24%	0.700
		4 Mil Core 0.5/0.5	4.000	3.84				4.000
12L-9		Copper	0.5		0	P	64%	0.700
		7.2 Mil Prepreg	7.200	3.63				6.416
12L-10		Copper	0.5		0	S	24%	0.700
		4 Mil Core 0.5/0.5	4.000	3.84				4.000
12L-11		Copper	0.5		0	P	64%	0.700
		3.6 Mil Prepreg	3.600	3.63				3.348
12L-12		CU Foil	0.25		1.1	S	100%	1.450
		Solder mask	0.500	4.20				0.500
		FINISHED PCB THICKNESS (mils)						63.260
		PCB thickness after Lamination						60.060
		# OF LAMINATIONS: 1						

12-layer stackup

Layer	Type	Thickness	Cop Wt	SE-50ohms Outer +/-15% Inner+/-10%	85ohms Outer +/-15% Inner+/-10%		100ohms Outer +/-15% Inner+/-10%	
				Trace Width	Trace Width	Spacing	Trace Width	Spacing
	Soldermask	0.5						
Top (L1)	Signal	1.9	1.5	4	4.8	7.2	3.9	13.6
	Prepreg	2.5						
Layer 2	GND	1.2	1.0					
	core	4						
Layer 3	Signal	1.2	1.0	3.5	4.5	6.5	3.5	13.5
	Prepreg	4.1						
Layer 4	GND	1.2	1.0					
	core	4						
Layer 5	Signal	1.2	1.0	3.5	4.5	6.5	3.5	13.5
	Prepreg	4.1						
Layer 6	GND	1.2	1.0					
	core	4						
Layer 7	Signal	1.2	1.0	4	4.9	8.1	3.7	15.8
	Prepreg	10						
Layer 8	GND / PWR	3.6	3.0					
	core	3						
Layer 9	GND / PWR	3.6	3.0					
	Prepreg	10						
Layer 10	Signal	1.2	1.0	4	4.9	8.1	3.7	15.8
	core	4						
Layer 11	GND	1.2	1.0					
	Prepreg	4.1						
Layer 12	Signal	1.2	1.0	3.5				13.5
	core	4						
Layer 13	GND	1.2	1.0					
	Prepreg	4.1						
Layer 14	Signal	1.2	1.0	3.5	4.5	6.5	3.5	13.5
	core	4						
Layer 15	GND	1.2	1.0					
	Prepreg	2.5						
Bot (L16)	Signal	1.9	1.0	4	4.8	7.2	3.9	13.6
	Soldermask	0.5						
	Total	94.8	+/-10%					

16-layer stackup

Sierra Circuits provides stackup design services. In case you need help, kindly send us your request.

The multiple metal layers in a PCB aid high connection density, minimum crosstalk, and good electromagnetic compatibility (EMC). These factors help in achieving good signal integrity. Ideally, all the signal layers should be separated from each other by ground or continuous power planes. This reduces crosstalk and provides uniform transmission lines with accurately controlled characteristic impedance. Efficient performance is achieved when using dedicated ground and power plane layers that are continuous across the entire board area. When it is not possible to implement ground or power planes between signal layers, care must be taken to ensure signal line coupling is minimized.

4.1.4 Lamination Selection

The dielectric materials used for laminations are discussed in this section.

FR4 Laminate

- Widely used in the electronic industry
- Economical
- Ideal for frequencies kept below 2.5GHz to 3GHz range
- Digital signal may be affected by the physical properties of the material

Rogers

- Dedicated high-speed laminates (Rogers RO4350)
- Used in RF applications

4.1.5 Stackup Design Material Parameter Considerations

The reason why a designer must choose the right material is stated below:

The velocity of a signal propagating through a printed circuit board is dependent on the dielectric constant of that board. For instance, when the signal frequency exceeds 5GHz, the typical dielectric constant of FR4, say around 4.7, drops close to 4. Whereas, the relative dielectric constant of Rogers remains constant – 3.5 from 0 up to 15GHz.

If the dielectric constant of the PCB changes with frequency, then different frequency components of the signal will have different velocities. This implies that these components will reach the load at different times. This leads to the distortion of digital signals. Along with this, the signal losses increase with the rise in frequency. This again will add up to the distortion of the digital signal.

4.1.6 Propagation Velocity

Electrical signals in the medium propagate slower than the speed of light in a vacuum. The speed is proportional to square root relative dielectric constant (E_r) of the medium.

$$V_{PROPOGATION} = (C_{VACCUM}/\sqrt{E_r})$$

Refer to the materials selection chapter for details on materials.

4.1.7 Planning High-Speed PCB Stackup

An accurately stacked PCB substrate will effectively reduce electromagnetic emissions, crosstalk, and improve the signal integrity of the product. A poorly arranged stack-up might increase EMI emissions, crosstalk and also the device becomes more susceptible to external noise. These issues can cause faulty operation due to timing glitches and interference which dramatically reduces the performance of the product.

With the right stack-up, the designer can suppress the noise at the source rather than correcting the issues after the product is built. PCBs involving multiple planes enable signals to be routed in microstrip or stripline controlled impedance transmission line configurations. The signals are tightly coupled to the ground or power planes and improve signal integrity by reducing crosstalk.

In high-speed PCBs, the ground and power planes perform three significant functions:

- Controls crosstalk amongst signals
- Deliver stable reference voltages for exchanging digital signals
- Distribute power supply to all the logic devices

While choosing a multilayer stack-up the designer should consider the following:

- A signal layer should always be placed right next to a plane.
- The signal layers should be tightly coupled (<10 MIL) to their adjacent planes.
- A power plane or a ground plane can be incorporated for the return path of a signal.
- Determine the return path of the signals. The high-frequency signals take the path of least inductance.

4.2 Selecting High-Speed Materials

The most common PCB material is FR4. This material is used in most electronic applications. However, when it comes to high-frequency signals, especially in the microwave domain, FR4 is not suitable.

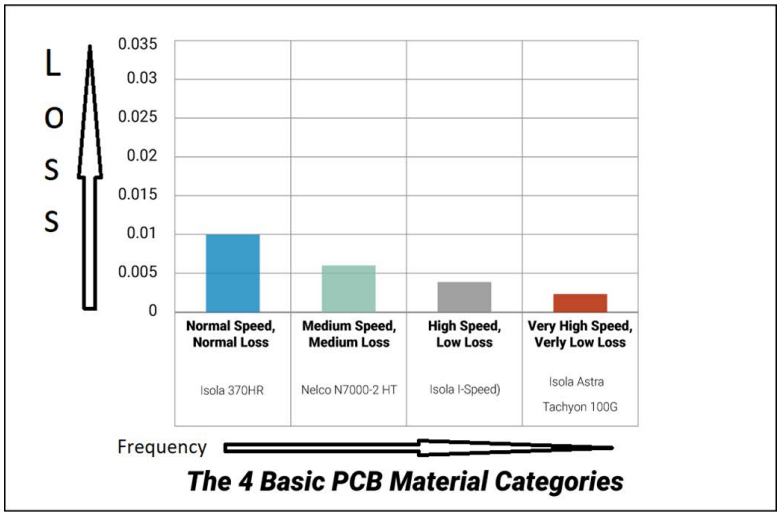
When designing PCB circuits at microwave frequencies, the key characteristics that define circuit laminate performance for microwave/RF printed-circuit boards include:

- Dielectric constant(Dk)
- Dissipation factor (Df)
- Coefficient of thermal expansion (CTE)
- Thermal coefficient of dielectric constant (TCDk)
- Thermal conductivity

The high-frequency material perhaps most familiar to users of PCB laminates is polytetrafluoroethylene (PTFE) which is a synthetic thermoplastic fluoropolymer that has excellent dielectric properties at microwave frequencies. Rogers materials are also commonly used.

4.2.1 PCB Material Categories

When selecting high-speed PCB laminates, what are the primary concerns that must be addressed in regards to manufacturability and cost? Let's take a look at this chart. For your convenience, we've classified important materials into buckets based on the materials' signal loss properties against a varying frequency range .



The 4 Basic PCB Material Categories

Normal speed and loss: Normal-speed materials are the most common PCB materials—the **FR-4 family**. Their dielectric constant (Dk) versus frequency response is not very flat and they have higher dielectric loss. Therefore, their suitability is limited to a few GHz digital/analog applications. An example of this material is Isola 370HR.

Medium speed, medium loss: Medium-speed materials have a flatter Dk versus frequency response curve, and have a dielectric loss about half that for normal speed materials. These are suitable for up to ~10GHz. An example of this material is Nelco N7000-2 HT.

Medium speed, medium loss: Medium-speed materials have a flatter Dk versus frequency response curve, and have a dielectric loss about half that for normal speed materials. These are suitable for up to ~10GHz. An example of this material is Nelco N7000-2 HT.

High speed, low loss: These materials also have flatter Dk versus frequency response curves and low dielectric loss. They generate less unwanted electrical noise compared to other materials. An example of this material is Isola I-Speed.

Very high speed, very low loss (RF/microwave): Materials for RF/microwave applications have the flattest Dk versus frequency response and the least dielectric loss. They are suitable for up to ~20GHz applications. An example of this material is Isola Tachyon 100G.

Exploring materials

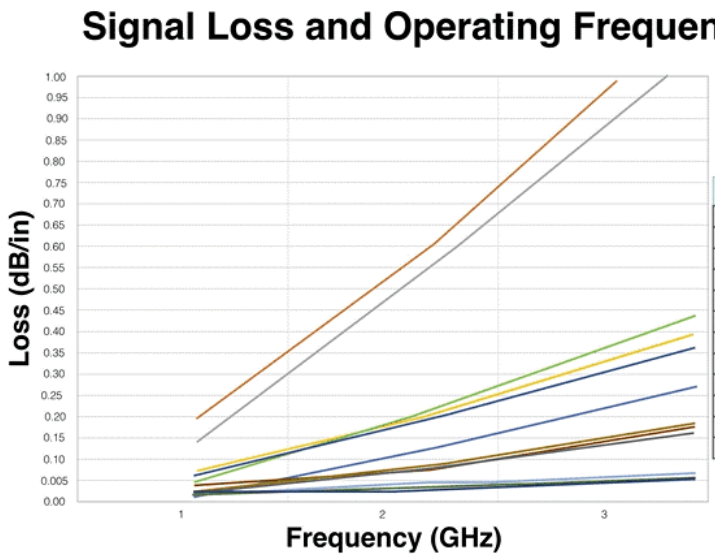
High Speed (500 MHz to 3 GHz)		
Manufacturer	Material Name	Application Areas
Isola	FR408HR	High Speed, Low Loss
Isola	I-Speed	High Speed, Low Loss
Panasonic	Megtron6 R-5775	High Speed, Low Loss

Low/Medium Speed (Below 500 MHz)		
Manufacturer	Material Name	Application Areas
Isola	FR370HR	Medium Speed, Normal Loss
Nelco	N7000-2 HT	Medium speed, Medium Loss

Very High Speed/ Microwave (3 GHz and above)		
Manufacturer	Material Name	Application Areas
Isola	I-Tera MT40	Very High Speed/Frequency, Very Low Loss
Rogers	RO3003	Very High Speed/Frequency, Very Low Loss
Rogers	RO4350 B	Very High Speed/Frequency, Very Low Loss
Isola	Tachyon-100G	Very High Speed/Frequency, Very Low Loss
Isola	Astra MT77	Very High Speed/Frequency, Very Low Loss

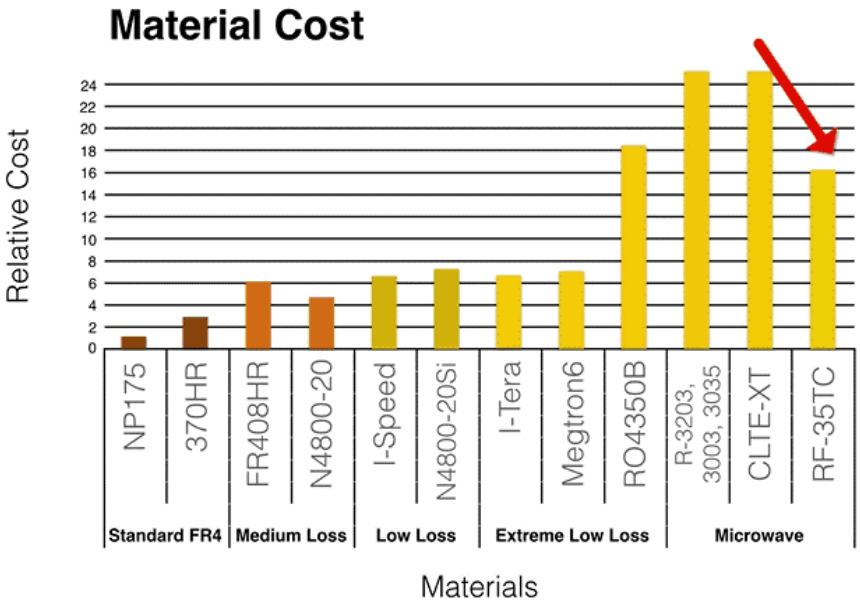
4.2.2 Signal Loss and Operating Frequency

What PCB material properties account for the difference in the PCB electrical performance, and how do these differences affect the PCB material cost? As it turns out, there are three main factors to evaluate when it comes to material performance for high-speed PCB designs. What is the signal loss at the operating frequency? Should you be concerned about the weave effect, and how easy is the material to manufacture your stack-up in construction?



Loss (dB/in)			
Freq (GHz)	2	5	10
370HR	0.19	0.6	1.1
NP175	0.13	0.55	1
N4800-20	0.067	0.2	0.37
N4800-20Si	0.0048	0.12	0.25
FR408HR	0.04	0.21	0.41
Ispeed	0.057	0.19	0.34
R4350	0.034	0.07	0.16
I-Tera	0.015	0.075	0.15
Meg-6	0.017	0.08	0.17
RF-35TC	0.018	0.019	0.047
R-3003	0.01	0.03	0.05
CLTE-XT	0.0095	0.04	0.047

First, let's take a look at the relationship between signal loss and operating frequency. As you can see from the graph, there's a direct correlation between signal loss and frequency. At the same time, we can also see that certain materials are less lossy than others. This was the basis we used to create our material classification bucket on the previous chart. This graph shows which materials could possibly perform better electrically at higher speeds.

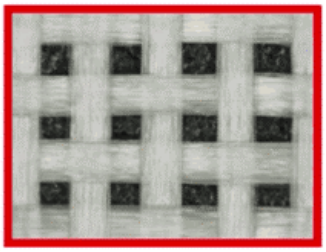


Next, let's compare the direct cost based on our material classifications. As you can see from the chart, less lossy materials cost more. You will have to decide what materials work best for your specific project. As you can see, the Rogers 4350B material is higher than that of Megtron 6 or Itera, even though electrical performance is similar. In the microwave category, the Taconic RF-35 is about 30% less expensive for the same performance as other materials in this category.

4.2.3 Non-PTFE Materials

Let's do a deeper dive into the non-PTFE materials. We will come back to the PTFE materials in a bit. Now, all of these materials perform somewhat similarly and at somewhat similar costs, but what justifies the cost differences, and what is the advantage of working with higher cost materials?

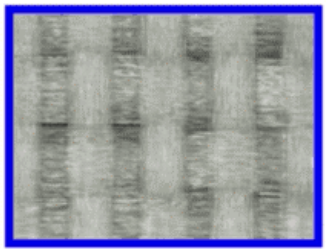
Loose Weave



Dk distribution is *un*even.

Thickness of the board varies widely.

Tight Weave



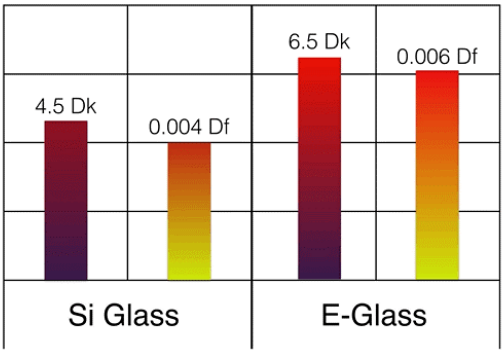
Dk distribution is even.

Thickness of the board does not vary.

First, we must understand material construction, and the effects of glass on characteristic impedance must also be understood. One way to achieve this is by understanding the weave effect and the different types of glass cloth. As you can see, different glass construction will affect DK distribution. A board with a loose weave will have greater variation in board thickness and greater variation in DK distribution. However, a tight weave will have a more consistent board thickness and more even DK distribution. The effective DK of the material remains the same as the signal traverses the dielectric.

What is really important to note from a manufacturing perspective is that a board with a tighter weave is easier to manufacture. When the glass weave is more consistent, mechanical laser drilling also becomes more consistent.

Si Glass versus E-Glass at 5 Ghz



Aside from the glass weave, there are two other types of glass to choose from, Si glass or E-glass. E-glass is the predominant glass type. E-Glass is a low alkali glass with a typical nominal composition of SiO2 54wt%, Al2O3 14wt%, CaO+MgO 22wt%, B2O3 10wt% and Na2O+K2O less then 2wt%. Some other materials may also be present at impurity levels. It varies the thickness between 1.3 mils to 6.8 mils. Looking at the chart, you can see the Dk of the E-glass at 5 gigahertz is 6.5, while the Df is .006. Now, Si glass is much purer than E-glass, and as a result, the Dk of 5 gigahertz for the Si glass is 4.5 and the Df is .004. The cost of the laminate compared to E-glass is about 15% higher.

4.2.4 Stackup Guidelines for Mixed Materials

Next, we will review three stack-ups and go over some basic stack-up guidelines for mixed materials.

- Stack-up #1 is a pure Rogers stack-up using Rogers 3000 materials. It is a multilayer construction that requires longer dwell times at higher temperatures. This lamination process is known as fusion bonding. Only a select few manufacturers, like Sierra Circuits, have the equipment and the expertise to perform this operation.
- Stack-up #2 is a hybrid stack-up using Rogers and Isola materials. Designers use this method to save on material cost and to aid in the manufacturability of multilayer stack-ups. Rogers is not suitable for sequential lamination process, and there are other material vendors, like Taconic and Isola, who make materials that perform similar to Rogers and do not have these limitations. In the past, it's been difficult to control the press-out thickness of these B-stage materials. Now, with better equipment, better process controls, customers can expect consistency and reap the benefits.
- Stack-up #3 consists solely of Taconic materials. These materials, although based on glass cloth, have similar performance to Rogers materials and are much easier to manufacture. With glass cloth, materials also become dimensionally stable.

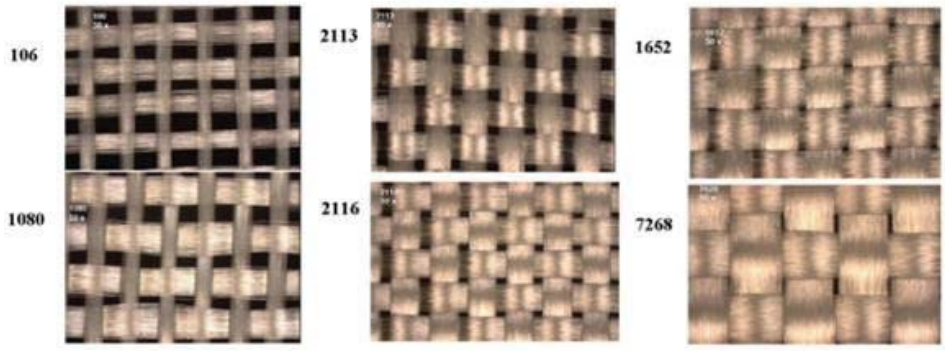
4.2.5 Hybrid Stack-up Guidelines

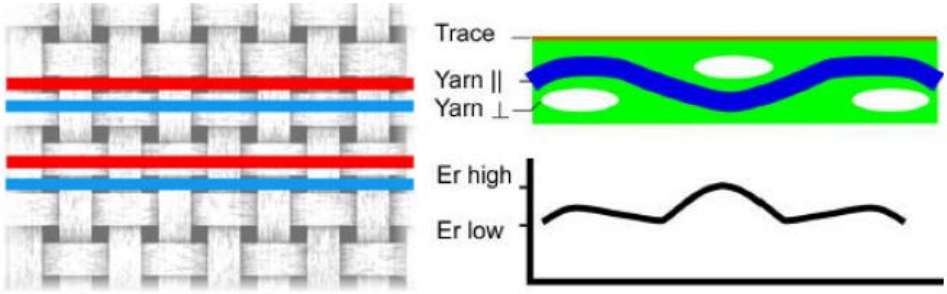
Now, let's discuss some hybrid stack-up guidelines. We recommend the following when Now, let's discuss some hybrid stack-up guidelines. We recommend the following when dealing with a hybrid construction. Use the high-performance material as the core. Laminate with FR-4 prepreg. Balance the FR-4 portion, and don't use a high Tg dielectric or bonding film with a lesser Tg material.

So, there you have it. We reviewed how to select high-speed materials based on performance and cost, including manufacturability.

4.3 Effect of Different Styles of Fibreglass Weaves on Impedance

The substrate of the PCB is made up of fibreglass material which is woven as a fabric and hardened with resin to make a flat enduring surface for a PCB. Different types to substrate have different weaves as shown below. Denser and closer the weave better and even the dielectric qualities. Thus, more uniform characteristic impedance. This results in better signal quality at high speeds.





When a set of high-speed differential signals are on the PCB, represented by the red and blue lines in the above figure, form a pair of differential traces. If you look closely, you will find that when one of the tracks is in the weaving space, the corresponding Er value will be greater than the other signal line, and the Er value is different. The result is change in the differential impedance. This phenomenon variation in impedance due to the dielectric layer glass weave is the fibre weave effect, and if weave density of sparser, its impact is more serious!

Common Fibreglass Weave Styles

Glass Style	Count Warp	Count per Inch	Warp Yarn	Yarn Fill	Glass Thickness
106	56	56	ECD-900 1/0	ECD-900 1/0	0.0015
1080	60	47	ECD-450 1/0	ECD-450 1/0	0.0025
1280	60	60	ECD-450 1/0	ECD-450 1/0	0.0022
2113	60	56	ECE-225 1/0	ECD-450 1/0	0.0029
2116	60	58	ECE-225 1/0	ECE-225 1/0	0.0038
3070	70	70	ECDE-300 1/0	ECDE-300 1/0	0.0034
1652	52	52	ECG-150 1/0	ECG-150 1/0	0.0045
7628	44	31	ECG-75 1/0	ECG-75 1/0	0.0068

Prepregs:

Generally, it is recommended not to use more than three different types of prepregs in a stack-up. The dielectric thickness of each prepreg layer should be less than 10 mils, otherwise, it increases the chance of a greater variation in the final thickness. Prepregs with very low-resin and high-glass content should be avoided. The low-resin content may lead to resin starvation during lamination. For example, 7628 and 2116 prepregs have low-resin and high-glass content.

4.4 Terms and Definitions for Stackup

- The dielectric constant (Dk) of a dielectric or insulating material can be defined as the ratio of the charge stored in an insulating material placed between two metallic plates to the charge that can be stored when the insulating material is replaced by vacuum or air. It is also called electric **permittivity** or **simply permittivity**.

  And, it is at times referred to as **relative permittivity**, because it is measured relatively from the permittivity of free space (ε0).

  The dielectric constant characterizes the ability of plastics to store electrical energy.

- The dissipation factor (tan δ) or Df is defined as the ratio of the ESR and capacitive reactance. The **dissipation factor** is a measure of loss-rate of energy of a mode of oscillation (mechanical, electrical, or electromechanical) in a dissipative system.

- The **coefficient of thermal expansion** (CTE) describes how the size of an object changes with a change in temperature. Specifically, it measures the fractional change in size per degree change in temperature at a constant pressure.

- Circuit materials are evaluated by a number of different parameters, including **dielectric constant** (D_k) and dissipation factor (D_f). Those two parameters also have temperature-based variants that provide insight into the expected behavior of a circuit material with changes in temperature, notably the thermal coefficient of dielectric constant (TCD_k) and the thermal coefficient of dissipation factor (TCD_f). The parameters detail the amounts of change in a material's D_k and D_f, respectively, as a function of temperature, with less change representing a material that is more stable with temperature.

5. EMI and EMC

EMC is the branch in electrical engineering that deals with the unintentional generation, propagation, and reception of electromagnetic energy. These elements may cause undesired effects such as electromagnetic interference (EMI).

In many designs, EMC design considerations are not taken during the initial design phase. Resolving the EMC issue after production can be a painful task. Most designers are under the impression that these problems can be fixed using additional EMC suppression components at the end of the product development cycle. However, this is quite challenging and can be an expensive fix.

5.1 Electromagnetic Compatibility (EMC)

A full treatment of EMI/EMC is outside the scope of this book. Here, we shall only talk of some good design practices that help towards reduction of generated EMI and greater immunity from received EMI.

5.2 What is EMC or EMI?

All electronic circuits generate electromagnetic interference or electromagnetic disturbance (EMI), and are also affected by EMI generated by other electrical/electronic equipment. Therefore, our goal during PCB design is two pronged:

- The product should not generate EMI disturbances exceeding acceptable levels.
- The product should be immune from acceptable levels of EMI disturbance.

If we achieve the two objectives above, we have implemented electromagnetic compatibility (EMC) successfully.

EMC standards specify both acceptable levels: EMI generation and EMI susceptibility. If a product is required to be EMC certifiable, then the design has to ensure that the product will operate such that generated EMI is within specified levels, and the product will not malfunction if specified levels of received EMI are present.
In the U.S., FCC governs the EMC regime; it classifies products in several categories – for business use (Class A) and for residential use (class B). Class B is stricter than class A.

5.3 Sources of EMI

- Radio frequency signals, harmonics, etc.
- Fast signal transitions, high frequency clock signals
- Transients generated by lightning, power circuits, motors, circuit breakers and other power switching devices, etc.

EMI can occur either by radiation or conduction:

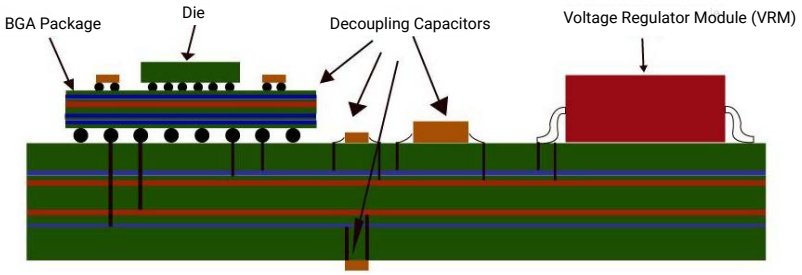
- Conductively through power input lines, cables, etc. This will be the predominant EMI below 30 MHz.
- By electromagnetic radiation from power and communication transmission lines, and power switching devices, arcing, and electrostatic discharges. These will be the predominant EMI above 30MHz.

5.4 Best PCB Design Practices for EMC

Proper grounding design practice:

- Majority of EMI problems can be traced to bad GROUNDING design. A good ground design will be less susceptible to EMI.
- Reduce current loops to minimum paying special attention to signal of high frequency. Current loops can be reduced by using solid ground references below high speed signals.
- Choice of logic family: do not choose a logic family faster than required; a faster logic family will generate more EMI.
- Choose the logic family with the highest noise margin; hence less susceptibility to EMI.
- Power rails are also a source of EMI problems. Use solid ground planes to avoid EMI issues.
- Impedance matching: signal ringing /distortion is less, hence less EMI.
- Shielding practice: Shield all very frequency circuit segments by metal enclosures.
- Filtering for EMC: low pass or band pass filters attenuate high frequency components:
    - A ferrite core inductor in series is an effective low-pass filter for input power rails: a ferrite bead has very high impedance at high frequencies and almost negligible impedance at low frequencies.
    - A capacitor in parallel
    - Mains filters
    - IO filters
    - Feedthroughs
    - Three terminal capacitors
    - Cable shield terminations

6. Power Integrity



6.1 Introduction - What is Power Integrity?

A circuit board requires one or more power supply voltages to operate. These are mostly generated by Voltage Regulator Modules (VRMs). These VRMs are designed to deliver the required maximum currents at the required voltages to the various devices on the circuit board.

Power Distribution Network (PDN) consists of all the interconnects from the VRMs to the terminals/pads of various components and devices (ICs, etc.) including all the bulk and ceramic decoupling capacitors, power and ground planes, the intervening vias, traces and the relevant leads, solder balls, wire-bonds, etc. of the device packages.

A PDN's any voltage rail is a single net but a very large one, having many components connected to it, and is spread over almost the entire PCB. **PDN is susceptible to electrical noise** generated by the components, and the various signal, power and ground nets on the PCB. Furthermore, faster and greater the number of the signal transitions (rise and fall times) switching over various I/Os and internal circuits of the devices on the board, greater will be the magnitude and frequency bandwidth of the electrical noise on the PDN.

PDN noise is injurious to the proper functioning of the board in several ways:

- When the magnitude of the noise on PDN exceeds a certain threshold, it alters the voltages delivered to the ICs below the acceptable values, causing malfunction of the circuits on the board.
- Even if a PDN supplies a voltage to the devices within tolerance, the PDN noise may still cause other problems. It can cause or appear as crosstalk on signal lines, it can transfer to the input power source line from where it can pass on to other VRMs inputs, thereby to their outputs.

- Furthermore, as PDN interconnects are usually the largest conducting surfaces on the PCB and carry the highest currents, any high frequency PDN noise has the potential of creating a lot of electromagnetic radiation, possibly causing failure to pass EMC compliance.

It is therefore important to control the PDN noise, and ensure that it delivers the required voltages within acceptable tolerance limits (usually within ± 2 to 5%), across the power supply voltage and ground terminals of the various devices mounted on the PCB, and the devices' dynamic current demands are met at all times and over their entire functional frequency range.

Power Integrity (PI) deals with all aspects of the PDN – it is designed to control the PDN noise.

6.2 PDN Block Diagram

Before we analyze the PDN in greater detail, let us look at a general PDN:

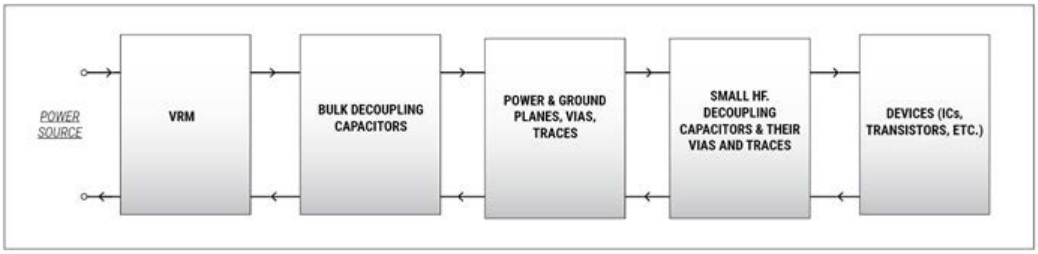


fig. PI-01. PDN Block Diagram

PDN starts from the various VRMs followed by bulk decoupling capacitors (usually electrolytic – aluminum/tantalum/polymer), power and ground planes with associated via and traces interconnects, multiple HF decoupling chip capacitors (usually ceramic capacitors) and the associated vias and traces interconnects to power supply voltage and ground pins of the various Devices – ICs, transistors, etc..

6.3 PDN Noise and its Causes

The control of PDN noise plays the most important role in ensuring good power integrity. In order to control it, one must first understand and analyze the causes and sources of the PDN noise.
If there were only constant DC current flow in the PDN interconnects from the VRMs to the ICs, that would cause a constant voltage drop, called the IR Drop, between the VRM and the ICs:

IR Drop = (Series resistance of the power and ground rails) X (Current in the rails) …… (PI-1)

However, the current drawn by the ICs and devices on the board is never constant but fluctuates rapidly with time. Thus, the current drawn is not DC but an AC current, and instead of 'IR' drop, we will need to consider the 'IZ' drop where Z is the AC impedance of the PDN network:

AC Voltage on PDN = (AC Impedance of the PDN) X (AC current in the PDN) ……………………. (PI-2)

In ICs and transistors, when the digital signals, either inside the IC chip and/or on the I/O pins and associated circuitry, switch from one logic level to the other logic level, the current drawn from the power supply pins of these devices also changes. This change occurs in a very short time characterized by the rise or fall time 'tr' which ranges from sub-nanoseconds to a few nanoseconds in high-speed circuits.

If ΔI is the amount of change in the current drawn by the IC from the power supply, and Δt = tr is the time during which this change occurs, then this change will induce a voltage Vnoise= L x (ΔI / ΔT) = L x (ΔI/ tr) across the power and ground pins, where 'L' is the inductance of the loop formed by the path of the power and ground nets i.e. the PDN. This noise voltage is rightly a cause of the PDN noise. There are three things apparent from this PDN noise source:

a. The greater the ΔI is, greater will the noise voltage be. So, if multiple signals, say 'n', are switching ***simultaneously*** in one or more devices on the same power rail, the current change in time 'tr' on that rail will be nΔI, so that noise voltage will become 'n' times:

$$V_{noisePDN} = L \times n \times (\Delta I / t_r) \quad \text{……………………………………………………………………………….. (PI-3)}$$

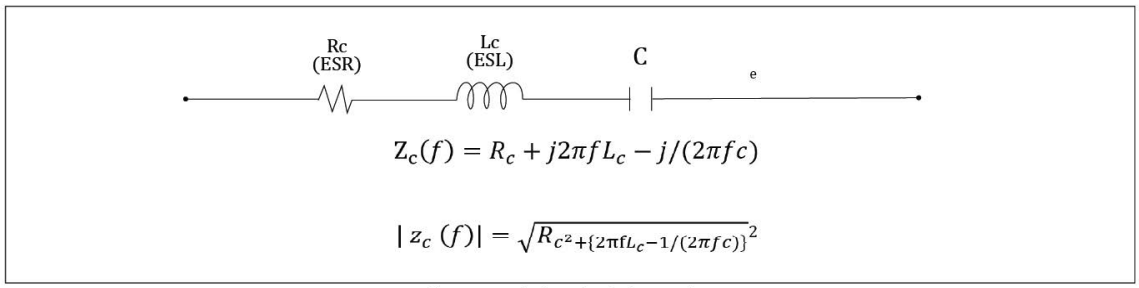
Complex ICs – FPGAs, microcontrollers, memories, ASICs, etc. – (i) have many I/Os and (ii) quite a lot of internal processing goes on inside them as per programs running therein. Both these sources result in switching taking place in a tremendous amount, and it would be very likely that a large number of signals are switching simultaneously, resulting in a large magnitude of PDN noise.

b. The smaller the value of 'tr', the greater will be the value of PDN noise. In our present era of ever increasing processing power occurring in shorter and shorter time durations in complex ICs and transistors, we are confronted with very high data transfer rates and extremely small rise times i.e. 'tr' – in the range of ***few tens of picoseconds***. Obviously, these devices have potential to create very high PDN noise.

c. Finally, greater the PDN inductance 'L' is, greater the PDN noise will be. What contributes to 'L' in the power delivery path? There are many sources:

i. Firstly, every loop in the PDN interconnect has a parasitic inductance proportional to its loop area. Thus, all the interconnects – inside the IC chip, from inside to IC terminals, from IC terminals to PCB pads, PCB traces and vias from pads to decoupling caps to power and ground planes and then to the VRMs – all form current path loops with inductances (usually in nH range).

ii. Secondly, the decoupling capacitors – both bulk electrolytic and ceramic types - are not ideal capacitors. They have inductances associated with their external and internal leads called ESL- the Equivalent Series Inductance - which can be several 10nHs in case of electrolytic capacitors and a few nHs in case of ceramic capacitors. Capacitors also have ESR – Equivalent Series Resistance – drop-through which adds to the PDN noise. The equivalent circuit of a real capacitor of stated value C is shown in the following diagram.



$$Z_c(f) = R_c + j2\pi f L_c - j/(2\pi f c)$$

$$|z_c(f)| = \sqrt{R_{c^2} + \{2\pi f L_c - 1/(2\pi f c)\}^2}$$

fig. PI-02. Equivalent Circuit of a Capacitor

Inductance of the capacitor increases its impedance at higher frequencies where it no longer functions as a capacitor. Every piece of conductor on the PCB and inside the components in the power delivery path has some parasitic inductance associated with it.

If we look at equation (PI-3), given the ICs and other active devices on the circuit board, the only thing in our control to limit the PDN noise is the PDN inductance L!

6.4 Analysis and Design of PDN

A circuit schematic diagram of the PDN network can be represented as follows:

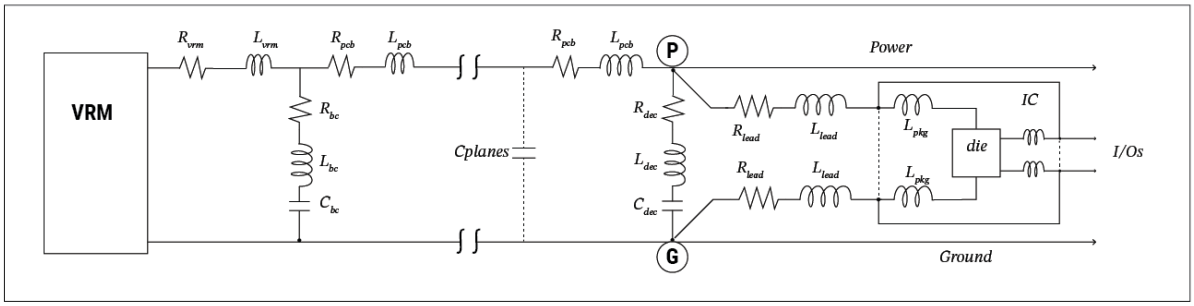


fig. PI-03. Equivalent Circiut Model of a typical PDN

The top and bottom lines represent the power and ground rails or planes. At P and G an IC is connected. This network comprises mainly VRM, resistors, inductors, and capacitors and its analysis is most conveniently done in ***frequency domain by circuit analysis techniques, either manually or by using SPICE***. What we need is to estimate the required **spectrum** of the frequencies of interest and look at the impedance ZPDN of the PDN network looking back from the points P and G where the devices – ICs and transistors – are connected to the PDN, and analyze how ZPDN varies with frequency over the bandwidth of interest.

6.4.1 Target Impedance ZPDN and its Frequency Spectrum

If I_{max} is the maximum current consumption rating of a particular PDN voltage rail – say of V_{CC} – then the actual current drawn by V_{CC} rail may vary, over a period of time, from very low to almost I_{max} depending on how many and how fast I/Os are switching simultaneously at a particular instant. If the fastest rise time is tr, then the highest frequency content in the current waveform is of the order of $f_m = 0.5/ t_r$, and it would be prudent to say that noise current waveform has a spectrum covering the frequency range from DC to f_m, and the magnitude Îm of a sinusoidal current waveform at any frequency of interest in this spectrum is $\leq \hat{I}_m = (1/2) I_{max}$.

If Z_{PDN} be the impedance of the PDN network at the frequency of interest, then the noise voltage generated on the V_{CC} rail will have a magnitude $\hat{V}_{Noise}$ given by:

$$\hat{V}_{Noise} = Z_{PDN} \times \hat{I}_m \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(PI-4)}$$

This noise voltage will occur as ripple voltage on the V_{CC} rail. In order that the ICs connected on the V_{CC} rail function properly, we need to ensure the $\hat{V}_{Noise}$ magnitude- does not exceed the acceptable ripple voltage of the IC's power supply voltage V_{CC} :

$$\hat{V}_{Noise} \leq \text{Acceptable voltage ripple} = V_{CC} \times \text{Acceptable Ripple\%} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(PI-5)}$$

Therefore, $Z_{PDN} \leq (V_{CC} \times \text{Ripple\%}) / (\hat{I}_m) = (V_{CC} \times \text{Ripple\%}) / (0.5 \times I_{max}) \ldots\ldots\ldots\ldots\ldots\ldots$ (PI-6)

We now define the Target Impedance - $Z_{T\text{-}PDN}$ - of the PDN network by:

$$Z_{T\text{-}PDN} = (V_{CC} \times \text{Acceptable Ripple \%}) / (0.5 \times I_{max}) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(PI-7)}$$

So that the actual PDN impedance should be limited by:

$$Z_{PDN} \leq Z_{T\text{-}PDN} \quad \text{(over the entire frequency spectrum of the PDN Noise Current) (PI-8)}$$

In the picture below we show a typical good PDN impedance plot vs Frequency and also the Target Impedance of the PDN. The actual impedance does go above the target impedance line for the entire frequency range from DC to 10GHz and that means that it meets the condition of the above equation (PI-8).

Thus, the design of a good PDN network involves the following steps:

(1) Determine the highest frequency $f_m = 0.5/ t_r$ where tr is the fastest signal rise or fall time. DC to a few f_m is the frequency range of interest.

(2) Calculate the target PDN impedance $Z_{T\text{-}PDN}$ for each voltage rail as per the above equation.

(3) Draw the PDN network or a simplified version of it, and calculate, using SPICE or manually, the actual PDN impedance at various frequencies i.e. to plot the PDN impedance spectrum (plot of impedance magnitude vs frequency), and to understand how various decoupling capacitors and geometry of the PCB conductors and vias in the PDN affect this spectrum shape.

(4) Choose appropriate decoupling capacitors and geometry of the PCB conductors and vias in the PDN to ensure that $Z_{PDN} \leq Z_{T\text{-}PDN}$ for each voltage rail over the entire frequency spectrum of interest.

Examples of calculation of fm and $Z_{T\text{-}PDN}$:

(1) **For V_{CC} = 3.3V rail,** Let the fastest rise time be 1ns. Therefore, the highest frequency is: $f_m = 0.5/ t_r = 0.5/ (1\ ns) = 500MHz$. Let I_{max} = 3A, ripple = 3%. Therefore, $Z_{T\text{-}Vcc}$ = (3.3V x 3%) / (0.5 x 3A) = 0.066Ω

(2) **For V_{DD} = 1.2V rail,** Let fastest rise time be 0.5 ns. Therefore, the highest frequency is: $f_m = 0.5/ t_r = 0.5/ (0.5\ ns) = 1000$ MHz. Let I_{max} = 1A, ripple = 2%. Therefore, $Z_{T\text{-}VDD}$ = (1.2V x 2%) / (0.5 x 1A) = 0.048Ω.

Generally, the target PDN $Z_{T\text{-}PDN}$ impedance falls in the range of 0.04Ω to 0.1Ω for most medium-to-complex requirements. And the frequency band of interest is DC to 1GHz. Thus, the Z_{PDN} magnitude should not go above $Z_{T\text{-}PDN}$ for the entire frequency band from DC to 1GHz. See the picture below as an example:

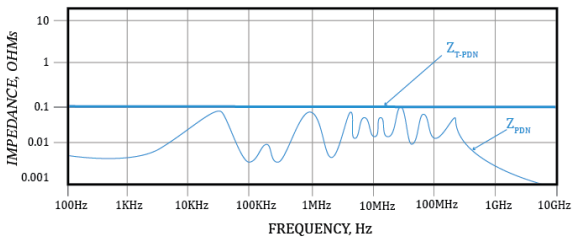
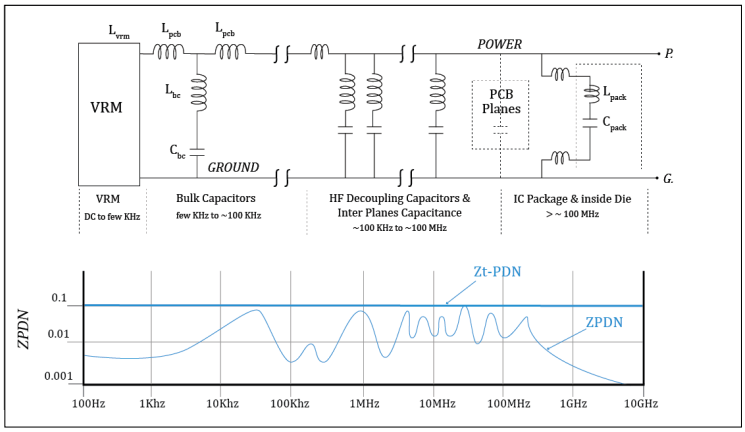


fig. PI-04. PDN Impedance vs. Frequency and Target Impedance

6.4.2 Estimation of Actual ZPDN over the Bandwidth

To estimate the actual PDN impedance at various frequencies, we need to analyze its equivalent circuit schematics model like the one shown in Fig. PI-03 above. The values of the resistors are quite small as compared to the impedances of inductances and capacitances; therefore a simplified schematics of a typical PDN network can be depicted as here under:



If we see the impedance of the above PDN looking back from P and G, we realize that the VRM, the bulk capacitors, HF decoupling capacitors, the IC package, and die play a very significant role in determining the magnitude of ZPDN in various frequencies zones. In PCB design, the IC package and die are not in our control, but the other elements are. We will therefore concentrate our analysis on the VRM, bulk capacitors, and the HF decoupling capacitors and their frequency zones of influence on PDN impedance.

6.4.2.1 Voltage Regulator Module (VRM)

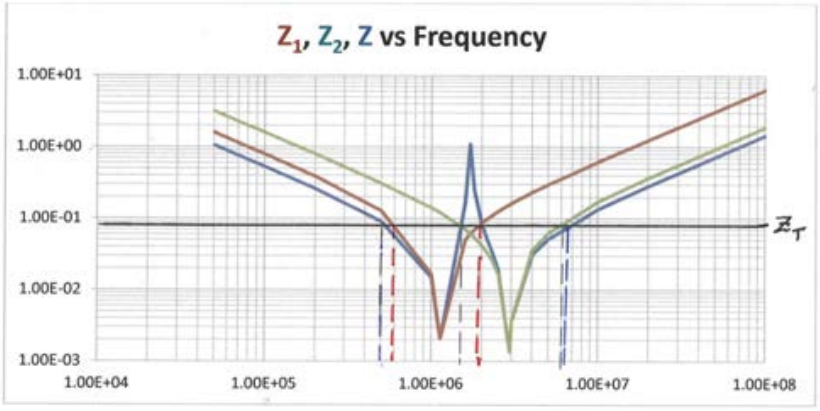
At low frequencies – from DC to about a few KHz, the VRM provides a low impedance for the PDN. The impedances looking back into VRM at 1kHz should be lower than $Z_T/2$. Generally, a well-chosen VRM will exhibit a very low impedance in this frequency range. For example, even for large value of $L_{VRM} \leq 3\mu H$, $Z_{VRM} \approx 2\pi f L_{VRM}$ would be $\leq 0.02\Omega$ at 1KHz frequency.

6.4.2.2 Actual Behavior of a Real Capacitor

If C, L_C, and R_C respectively are the capacitance, Equivalent Series Inductance (ESL), and Equivalent Series Resistor (ESR) of a real capacitor, then the impedance Z_C will have a minimum value = ESR at the resonant frequency given by:

$$F_r = 1 / (2\pi \times \sqrt{Lc \times C}) \quad \text{..... (PI-9)}$$

If we plot the impedance Z_C of a single capacitor versus frequency, we get a plot similar to one shown by the red and green curves for the capacitors C1 and C2 respectively in the following diagram. Note that for frequency < F_r, the impedance is effectively capacitive (i.e. impedance decreases as frequency increases) and for frequency > F_r, it is inductive (i.e. impedance increases with frequency). If we also draw the target impedance Z_T line in this diagram, this line cuts the Z_C line at two frequencies; and within the frequency range given by them, we find that $Z_C \leq Z_T$. We thus know over which frequencies the given decoupling capacitor will be useful in keeping the PDN impedance within target.



C_1 = 2uF, L_{c1} = 10 nH, $F_{resonance\text{-}C1}$ = 1.13 Mhz : C_2= 1uF, L_{c2}= 3nH, $F_{resonance\ (C2)}$= 2.91 MHz

C = C_1 II C_2, Addnl. Third High Resonance Frequency = 1.71 Mhz.

FIG. PI-06. Impedance of Individual and Composite (parallel) Capacitors vss Frequrency

In the above diagram, we have also shown the case of two capacitors. Red line corresponds to C_1, the green line corresponds to C_2, and the blue line corresponds to the effective combined C= 'C_1 in parallel with C_2'. ***We see that for the combined C, there is a impedance peak exceeding the Z_T line at a frequency lying in between the two resonant frequencies $F_{r\text{-}c1}$ and F_r-c_2.*** **The height of this peak is found to be inversely proportional to the ESRs value; therefore very low ESR values can sometimes be counterproductive in keeping Z_{PDN} below Z_T.** One of the ways to remove this peak is to introduce a third capacitance whose resonant frequency lies between the two resonant frequencies; though we will now have 3 valleys and 2 peaks, still the magnitude of the peaks will be lowered as a result of the low impedance of the third capacitor in that frequency range.

If we use multiple capacitors of the same value in parallel, we may have multiple peaks but they will be close together and their magnitudes will be small. Using 'n' exactly similar capacitors in parallel has the effect of increasing the effective value of capacitor 'n' times while dividing the value of ESL and ESR by 'n'. However, if we have 'n' dissimilar capacitors in parallel, the equivalent impedance plot will have, in addition to 'n' minimum valleys, also 'n-1' peaks, and we need to be careful while choosing the capacitors so that the peaks do not go above the $\mathbf{Z_T}$ line.

6.4.2.3 Role of Bulk Capacitors

These are typically electrolytic capacitors – aluminum, tantalum or polymer types. Their resonant frequencies range - $\mathbf{f}_{bclow}$ to $\mathbf{f}_{bchigh}$ - from a few kHz to 100kHz, and they are thus able to keep the PDN impedance low in the frequency range from a few kHz to 100kHz. Their ESL is of the order of 10 to 20nH. The bulk capacitance value is so chosen in orders to make the impedance of bulk capacitor < Z_T at 1kHz.

Guidelines for choosing bulk capacitors:

Let Z_T be the PDN target impedance.

1. Do not choose a tantalum capacitor with very low ESR value as it may cause unwanted high peaks when the effect of other capacitors in parallel - tantalum as well as ceramic - is also taken into account. Choose a tantalum capacitor with ESR ≈ 0.5 Z_T .

2. As the effective frequency range of tantalum capacitors is ~ 1kHz to 100kHz, choose the capacitor value C such that its impedance (1/(2πfC)) at f_{bclow} = 1kHz is less than $\sqrt{(Z_T^2 - ESR^2)}$.

$$C_{bulk} \geq 1/[\,2\pi f b_{clow}\ \sqrt{(Z_T^2 - ESR^2)}\,] = 159/\sqrt{(Z_T^2 - ESR^2)} \quad \ldots\ldots\ldots\ldots (PI\text{-}10)$$

Example: If Z_T = 0.1Ω, ESR = 0.05Ω, $\mathbf{f}_{bclow}$ = 1kHz, then, $C_{bulk} \geq 159/\sqrt{(0.1^2 - 0.05^2)} = 1836$ µF

So, a bulk capacitor of 1840µF with an ESR ≈ 0.05Ω will be required.

ESL of a typical high value tantalum capacitor is ~ 20nH.

It will be difficult to find a tantalum or polymer capacitor of capacitance near 1800µF with an ESR of 0.05Ω. So, it would be best to use 2 or more tantalum capacitors in parallel.

We could use 2 capacitors of 1000µF, ESR=0.1Ω so that effective C= 2000µF & ESR = 0.05Ω ohms.

Or, we could use 4 capacitors of 470µF, ESR = 0.2Ω each, so that effective C=1880µF and ESR= 0.05Ω.

Or, we could use three tantalum capacitors: two – C_1 and C_2 - each of 680µF and ESR = 0.2Ω each and one C_3 of capacitance = 500µF, ESR = 0.1Ω. As this case involves dissimilar capacitors, we will go for this here. Parallel of two similar capacitors - C_1 II C_2 - gives effective capacitance = 1360µF and effective ESR = 0.1Ω. Let C= C_1 II C_2 II C_3 be the final capacitance (≈1860µF, ESR =0.05Ω). The plot of Z_C will look like as under:

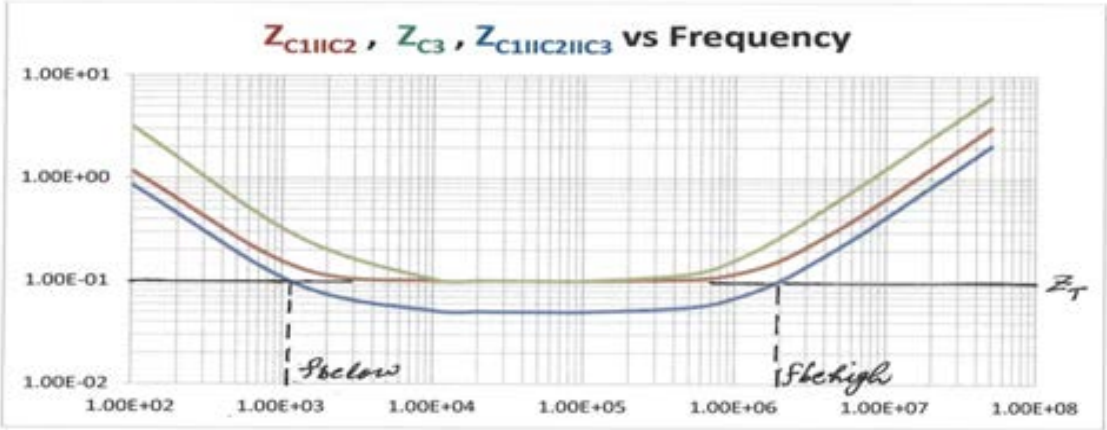


FIG. PI-07. Impedance vs. Frequency of Three Tantalum Capacitors in Parallel.

We see that the impedance is less than o.1Ω for 1kHz to 2MHz.

3. We can now estimate the $\mathbf{f_{bchigh}}$, the highest frequency at which the bulk capacitor impedance will be $\leq Z_T$. At this frequency, the impedance will be effectively inductive in series with ESR. This frequency will be:

$$f_{bchigh} = \sqrt{(Z_T^2 - ESR^2)} / (2\pi ESL) \quad \text{(PI-11)}$$

= 0.0866/(2π x 6.67nH) ≈ 2.1 MHz in this example as also indicated in the plot above.

As we had indicated, bulk capacitors are to ensure $Z_{PDN} \leq Z_T$ in the frequencies up to a few 100kHz, correctly speaking upto f_{bchigh}. Above f_{bchigh} or 100kHz, whichever is higher, the bulk capacitors will behave highly inductive and their impedance magnitude will be $> Z_T$, therefore we need high frequency decoupling capacitors like ceramic chip capacitors to control the impedance of the PDN.

6.4.2.4 Ceramic Chip Decoupling Capacitor

Ceramic chip capacitors, also called as MLCCs, have resonant frequencies in the range of a few 100kHz to a few 100MHz (depending on value and size) and they have very low ESRs – of the order of a few milliohms to few 10s of milliohms. They play the dominant in controlling the PDN impedance and keeping the PDN impedance ≤ target impedance in the frequency range of 100kHz to 100MHz. These capacitors are very small SMT components – their individual capacitances range from a few Pico-Farads to tens, and even hundreds of Micro-Farads.

A 0.001µF ceramic capacitor typically has a resonant frequency of ~ 300MHz (0201 size) to ~200MHz(0805).

A 0.01µF ceramic capacitor typically has a resonant frequency of ~90MHz (0201 size) to ~70Mhz(0805 size).

A 0.1µF ceramic capacitor typically has a resonant frequency of ~30MHz (0201 size) to ~20Mhz(0805 size).

A 1µF ceramic capacitor typically has a resonant frequency of ~10 MHz (0201 size) to ~ 6MHz (0805 size).

A 10µF ceramic capacitor typically has a resonant frequency of ~3MHz (0402 size) to ~ 2MHz (0805 size).

Guidelines for choosing ceramic capacitors:

If we continue the example given above for tantalum capacitors, we find that tantalum capacitors are able to control the $Z_{PDN} < Z_T$ upto $f_{bchigh} = 2MHz$. Above 2MHz, ceramic capacitors control the PDN impedance.

At 2MHz, we require a ceramic capacitance value given by: (ZT=0.1Ω , ESR of capacitor = 0.04Ω)

$$C_{cer} \geq 1/[\,2\pi f_{bchigh} \sqrt{(Z_T^2 - ESR^2)}\,] = 1/\,(2\pi 2x10^6 x\ 0.0916) = 0.87\mu F \quad \text{.....(PI-12)}$$

This value is in the range of 0.1 to 1µF; its resonant frequency will be about 10 to 30MHz as per earlier data.

At 100MHz, the impedance of this ceramic capacitor will be largely inductive. We want the this inductive impedance to be $\leq \sqrt{(Z_T^2 - ESR^2)} = 0.0916\Omega$ **at 100MHz; so that the inductance - ESL is limited by:**

$$ESL_{cer} \leq \sqrt{(Z_T^2 - ESR^2)} / (2\pi f_{cerhigh}) = 0.0916/(2\ \pi\ x\ 100\ x\ 10^6) = 0.146nH \quad \text{.....(PI-13)}$$

It would be more than safe to assume an effective ESL = 1nH per ceramic capacitor. Therefore, to keep ESL < 0.146nH, we require at least 1nH/ 0.146nH = 7 capacitors in parallel. As the total value required should be ≥ 0.87µF, each capacitor should have a value = 0.87/ 7 = 0.124µF.

The nearest available standard value is 0.1µF. They have a typical ESR = 0.04Ω. So, we will require 9 such capacitors in parallel. There effective ESL will be 1nH/9= 0.11 nH, and effective ESR will be 0.04/9 = 0.0045Ω. These will result in the Z_{PDN} at 100MHz = $\sqrt{((2\pi fL)^2 + ESR^2)} \approx 0.07\Omega$, well within the Z_T limit. In fact, these will keep the Z_{PDN} within Z_T limit for up to 145MHz.

In this way, one can decide on the value and number of ceramic capacitors required to keep the PDN impedance below target for frequencies up to 100MHz or even higher.

The most widely used ceramic decoupling capacitors are of values 0.1µF. To extend the low PDN impedance range beyond 100MHz, one uses capacitors of values 0.01µF (=10nF=10,000pF) Z_T limit and 0.001µF (=1nF=100pF).

One thing that we should look out when paralleling different value ceramic capacitors. This was discussed in section 2.4.4.2.2 (Actual Behavior of a Real Capacitor) above. Do not choose two different values only; choose 3 different values to avoid high resonant peaks.

These decoupling capacitors are installed on the PCB very close to IC power and ground terminals so that parasitic trace inductance from capacitor pad to the IC terminal pad is very low. The inductance of the vias from the power and ground planes needed to connect to the capacitor terminals also add to the overall inductance of the capacitor. Thus, we need to take into account not only the ESL of the chip capacitor but also the loop inductance of the vias and the traces that connect the IC's power and ground pins to the capacitors and to the power and ground planes.

6.4.2.5 Trace Loop Inductance

Trace loop inductance is given by :

$$L_{lptr} \approx Z_{ch} \times T_{pd} = Z_{ch} \times l \times t_{pd} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (PI\text{-}14)$$

Here Z_{ch} is the characteristic impedance of the trace loop, 'l' is the length of the trace and t_{pd} is the propagation delay per unit length, which depends on the effective dielectric constant E_{reff} of the PCB material.

To keep it low we need to make 'l' as well as 'Z_{ch}' low. Hence, we can formulate the following design rules to keep traces loop inductances low:

1. Keep 'l' length as short as possible. Place decoupling ceramic capacitors as close to the IC as possible.

2. Keep the width of the traces as wide as possible. This will keep Z_{ch} low.

3. Keep the height between the component layer and ground and power planes as low as possible. This will also keep Z_{ch} low.

6.4.2.6 Via Loop Inductance

For a pair of vias (of height h, via diameter d, and center to center distance D), the via loop inductance L_{via} is given by:

$$L_{vp} \approx 0.4 \times h \times [\ln(2D/d) + 1/4]\ nH \quad \text{..... where h is in mm. ..... (PI-15)}$$

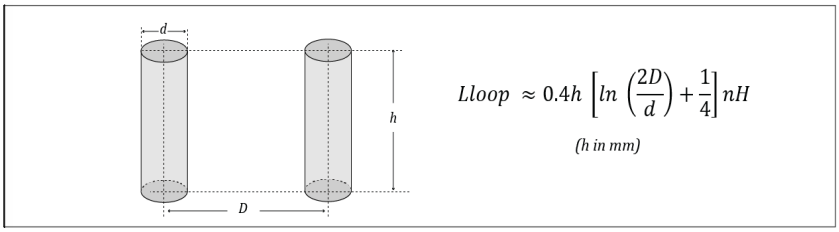


fig. PI-08. Loop Inductance of Vias

Example: 8mil 'd' via, with D = 40mils and h = 60mils = 1.5mm, L_{vp} = 1.53nH.

6.4.2.7 Planes Loop Inductance

If w is the width, l the length and h the separation between two planes, the loop inductance is given by

$$L_{ploop} = (1.28\ h\ l\ /\ w)\ nH;\ h \text{ is in mm.} \quad \text{..... (PI-16)}$$

Example: If l = 5, w and h = 10mils = 0.25mm, L_{plane} = 1.6nH.

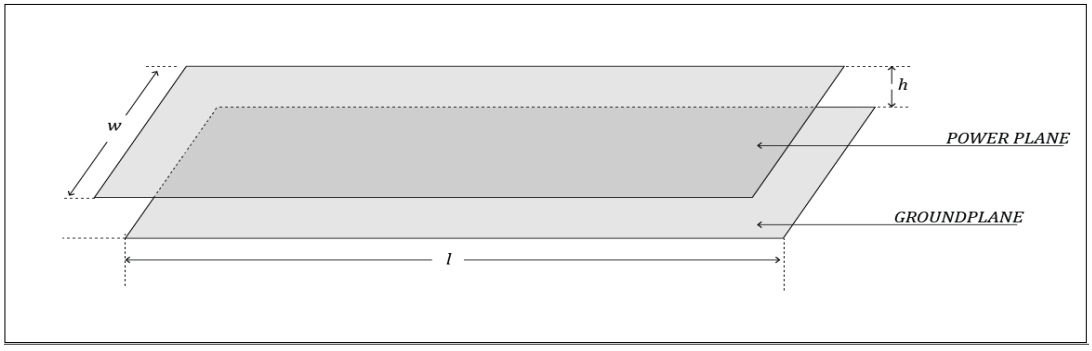


fig. PI-09. Loop Formed by Power & Ground Planes

All the above come into play when considering the total inductance in the path of IC power supply ground pins connections to the power and ground planes and the decoupling capacitors.

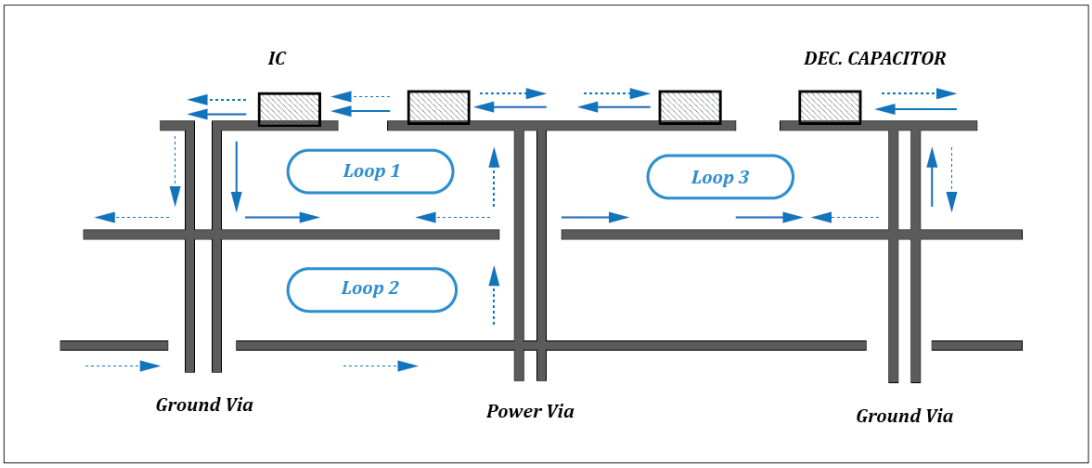


fig. PI-10. Inductance Loops of an IC & Capacitors

In the above example, the IC and decoupling capacitor connections to the ground and power planes are shown.

Loop 1 and Loop 3 are via loops, Loop 2 is a plane loop or via to plane spreading loop.

6.4.2.8 Spreading Loop Inductance

Spreading loop inductance between two vias (diameter 'd') with separation 'D' in the loop of two planes of vertical separation 'h' is given by

$$L_{via\text{-}via} = 0.84\ h\ ln(D/d)\ nH;\ h \text{ is in mm.} \quad \text{..... (PI-17)}$$

The overall inductance in the above scenario of a decoupling capacitor can be of the order of a few nH as compared to ~1nH for the internal ESL of the capacitor.

To keep via related inductance low, we should use the following rules:

i. Design vias with larger diameters
ii. Keep the distance between vias small
iii. Keep the height of vias and the distances between power and ground planes small

6.4.2.9 Capacitance of a Pair of Planes

Inherent capacitance between power and ground planes plays an important decoupling role at high frequencies to keep the PDN impedance under control.

Capacitance between two planes (like shown in figure PI-9 earlier) is given by

$$Cplane = €_{ref} f\ 225\ (A / h)\ pF \quad \text{..... (PI-18)}$$

Where A is the area of the coupling planes in square inches, h is the separation height in mils in between the planes, and $€_{reff}$ is the dielectric constant (or relative permittivity) of the dielectric material between the planes.

Example: If A = 4" x 6" = 24 sq." and h = 4 mils, and €r = 3.8, then

C_{plane} = (225 x 3.8 x 24) x 4 = 5130pF = 5.13nF.

If we calculate the inductance of these planes loop as per equation PI-16, we get:

L_{ploop} = 1.28x(4/40) x 6/4 = 0.192nH.

This gives the resonant frequency of the planes as:

f_{r_planes} = 1/(2π√(LC)) = 160MHz.

So, this will play a useful role in the frequency range of 100 to 200MHz.

6.4.2.10 IC Package and Internal Die

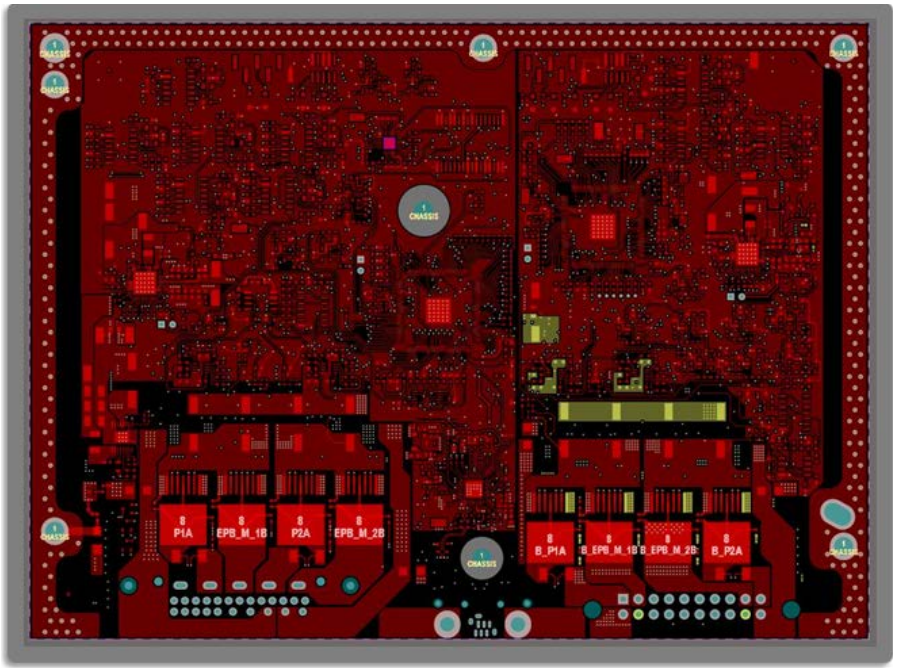
Beyond a few 100MHz, the parasitics inside the IC package and inductances and capacitances in the semiconductor die dominate in determining the Z_{PDN} and they practically limit the safe highest frequency beyond which the IC should not be used. However, control of this is beyond the scope of the PCB designer, so we shall not go into further details of this topic.

6.5 Power Integrity, Signal Integrity, and EMI are related

We observed that in order to keep ZPDN within control, we need to keep the dielectric height low between a ground plane and components, and also between power and ground planes. This is also required to reduce crosstalk and maintain good signal integrity. Thus, good power integrity also leads to better signal integrity. Furthermore, if noise on the PDN is controlled, then the PDN noise coupled onto signal nets will also be reduced and furthermore EMI will also be controlled.

7. High-Speed PCB Layout Design

The high-speed board layout design requires careful planning of footprint design, component placement, and routing of the traces. This chapter discusses the essential layout design requirements in a high-speed design.



7.1 Footprint Design for High-Speed Boards

7.1.1 Component Footprint Shapes

During a PCB design, a lot of thought is put into the schematic organization, board materials, layer configuration, critical component placement, and routing of high-speed signals. But one thing doesn't get as much attention as the rest of the design aspects is the footprint shapes. Although the components used in the high-speed design aren't much different from the conventional design, there are some minute changes that can help in creating a high-speed design.

7.1.2 Pad Shapes for High-Speed PCB Design

In high-speed design, the primary thing to consider during the evaluation of footprint shapes is the size of the footprint pad shapes.

The pad shapes are the bare metal pads where the component pins will be soldered to once the PCB is manufactured. Generally, some of the pad shapes are replicated to produce an entire component footprint shape. Approximately, the PCB pads are 30% larger than the pins. The pad sizes are carefully calculated considering the manufacturing issues that could arise during the fabrication process. Issues like tombstoning, where the surface mount devices like capacitors and resistors flip up one side can ruin the functionality of the board. With the right pad size, these kinds of issues can be resolved with manual rework.

Despite all these benefits, for a high-speed design, the extra metal can increase parasitic capacitance and increase the connection length between critical components. In order to suit the high-speed needs, the pad sizes must be reduced to avoid the parasitic capacitances. Instead of enlarging the pad size by 30% of the actual pin size, it would be beneficial to increase it only by a small margin of 5%.

Additionally, the connection lengths can be reduced by decreasing the spacing between components. Implementing smaller pad sizes does not affect the mechanical strength since the contact area between the pins and the PCB remains the same. Smaller pads occupy less space on the board but the manufacturing cost goes up. The designer should understand the manufacturing capabilities of a PCB manufacturer before reducing the footprint pad sizes.

Another design technique that can help in high-speed design is rounding the corners of the pads. Incorporating rounded pads will enable the designer to route traces closer to the pads. This will reduce connection lengths creating a compact circuitry.

7.2 Component Placement

7.2.1 Component Placement Strategy

The systematic placement of components plays a prominent role in high-speed PCB design. Here are some strategies to consider for high-speed circuits.

7.2.2 Floor Planning

The first step in PCB layout design is to have a floorplan. A floorplan is a sketch that allocates general areas where blocks of circuitry are to be placed on the board.

7.2.2.1 Wonders that a Floorplan can do

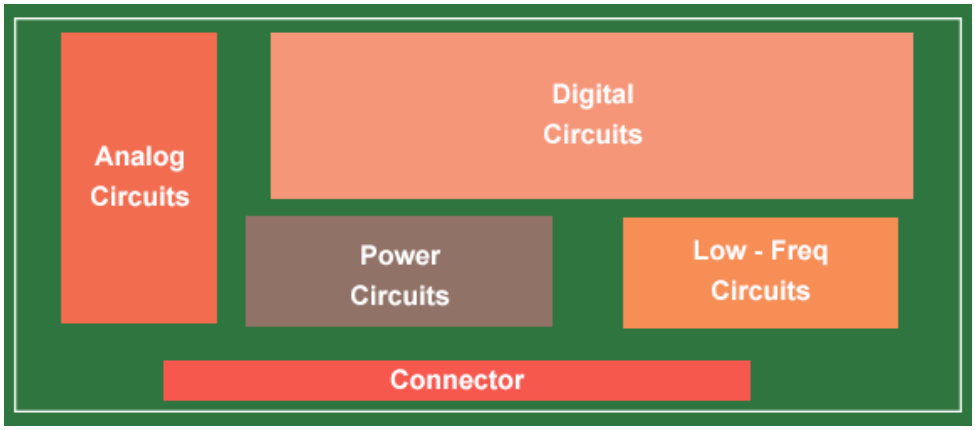
The floorplan links the schematic drawing and the layout. It provides a head start to the designer on component placement. A pre-placement floorplan will allow the designer to optimize the component placement for signal integrity goals. Also, the small components, like bypass capacitors and termination resistors, will be placed at an early stage instead of getting squeezed into the design at the end. The functional blocks of circuitry like power conditioning, RF, digital, analog, etc., should be arranged as groups to reduce signal crossing.

A floorplan gives an insight into how the signals flow between functional blocks. For an efficient board, group the power conditioning together so that their signals do not have to cross through sensitive areas of RF circuitry. Plan your placement to maintain the connection lengths as short as possible. The components that are part of high-speed signal paths where multiple nets connect a series of components should be placed as close together. The designer has to consider the routing channels while planning the component placement to ensure there is adequate space. The requirements of power and ground planes should also be considered when planning out the placement of functional blocks of circuitry.

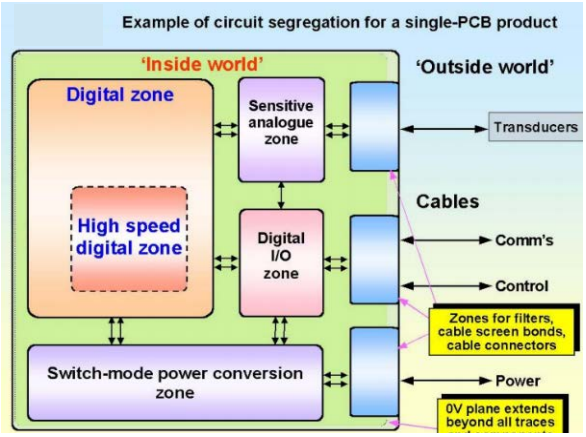
Always implement continuous power planes unless there is a scenario where the design demands a split power plane. When dealing with split power planes, be cautious while placing the connected components across the split. The high-speed transmission lines should not cross the splits in power planes since it will break up the return path for those signals. Finally, avoid placing components of a different functional group in the midst of another circuit. Even this will affect the return path of the circuit.

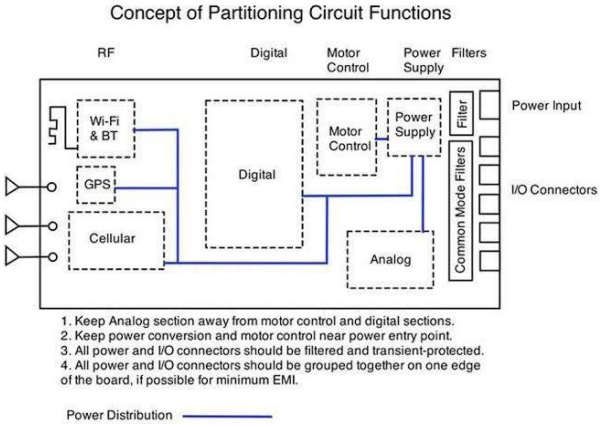
7.2.2.2 Component Placement Considerations in High-Speed PCBs

As a first step, the designer should read the schematic and breakdown into sub-sections depending on the circuit function. For instance: analog, digital, high-speed, high-current, power supply, etc..



Apart from the circuit function, the voltage and current levels should be analyzed. Circuits with similar VCC and GND should be grouped and placed together.





Refer to the schematic circuit diagram while placing the components. Identify the main components of the circuit such as microprocessors, ethernet chips, memories etc. Place these as per the floorplan and with shortest traces between these main chips as per the datasheet guidelines and which makes the signal flow smooth and unidirectional as far as possible. Next, place the components associated with the main components such as crystal oscillators, decoupling capacitors, termination resistors.

Some of the component placement considerations are discussed below.

- To begin with, avoid placing sensitive high-speed devices close to the edge of the board. This is because the edge of the board possesses different impedance characteristics and also there is a higher chance of electromagnetic interference (EMI). On top of this, connectors that connect the PCB can radiate EMI. In view of these factors, it will be a good practice to place sensitive high-speed devices close to the board center to reduce the influence of EMI.

- The thermal effect is another crucial aspect to be considered. In high-speed boards, the devices may run at a higher temperature than standard board components. To ensure that these hot components stay cool, implement a placement strategy in which these components receive an unrestricted airflow. For instance, do not place bigger components like connectors in the path of airflow to a hot BGA.

7.2.3 Termination Resistors

In high-speed PCBs, the termination resistors must be placed along with the rest of the components instead of squeezing them in the end. These resistors are usually addressed at the end once the main parts of the circuitry have been placed. Since termination resistors are part of the circuit as a whole, their placement is critical for the accurate operation of the circuit.

Here are two commonly used schemes for placing termination resistors:

Simple parallel termination:

A termination resistor is placed on the end of the circuit nearest to the receiver while the other side is attached to power or ground plane. The greater the trace length from the load pin to the resistor, the higher the circuit susceptible to signal reflection. Hence, the designer should place the resistor as close as possible to the load pin of the receiver to minimize the stub length of the connecting trace.

Series termination:

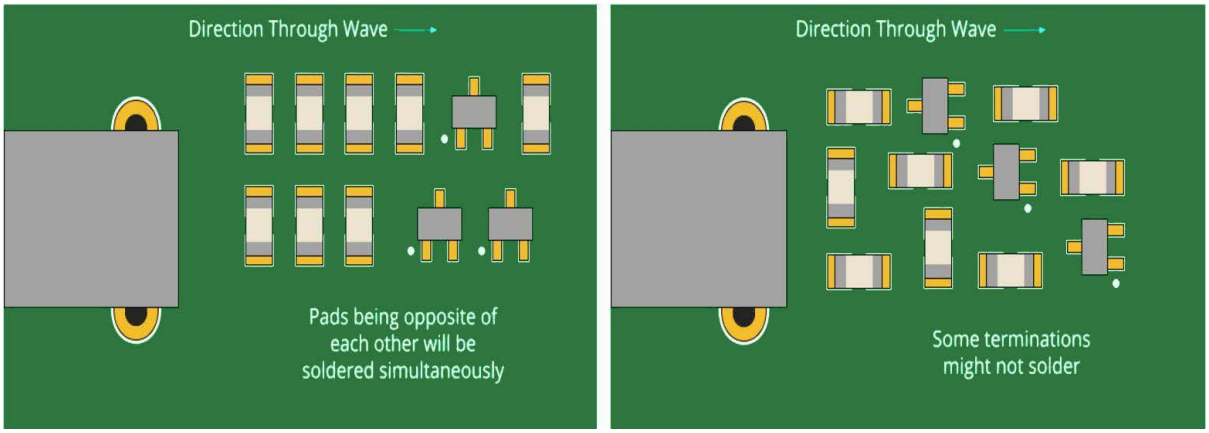
The series resistor is attached inline immediately after the driver pin of the circuit. Since the resistor is an inline part, it doesn't have the stub length to be considered like in a parallel termination resistor. After figuring out the right strategy for placing the termination resistors, the designer can include it in the floorplan.

In view of the above strategies, along with circuitry path and power and ground requirements, a commendable design can be drafted for high-speed layouts.

While the whole component placement process is challenging, the way in which it is done will determine the manufacturability of the boards.

7.2.4 Component Orientation

Align similar components in the same direction. This helps in effective routing in PCB design and ensures an error-free soldering process during assembly.



Good Components Orientation (left) and Poor Components Orientation (right)

7.2.5 SMT and Through-Hole Component Placement

It's advisable to place all the surface mount devices (SMD) on the same side of the board. All through-hole components should be placed on the top side of the PCB to reduce the assembly steps.

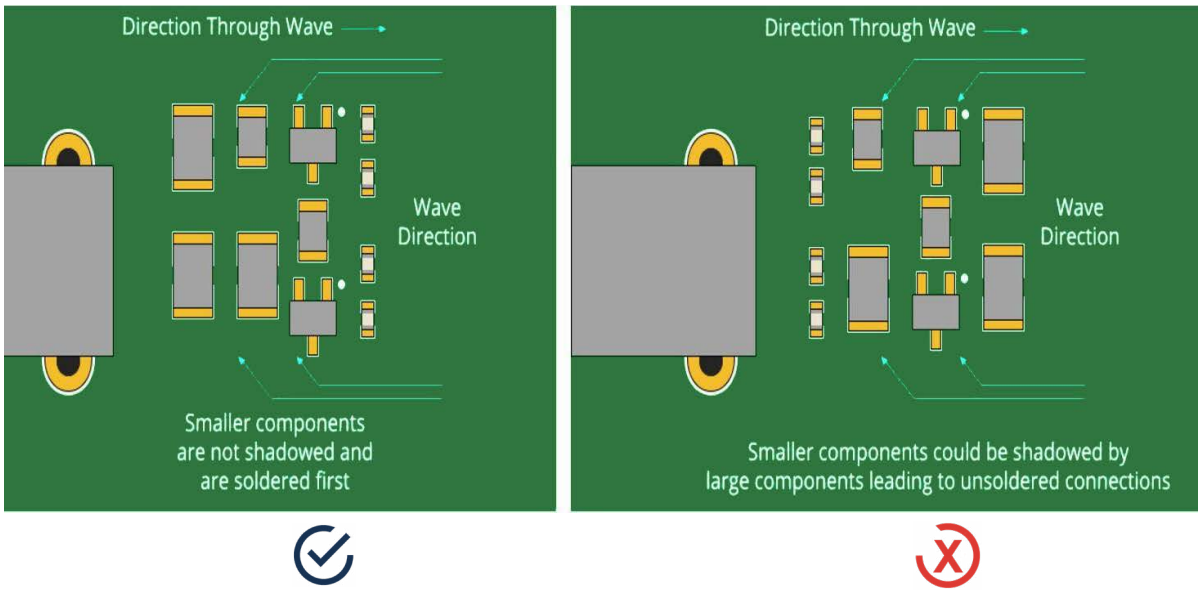
7.2.6 Via Shapes Considerations

In a high-speed circuit, any mental on the PCB should be considered as part of that circuit. The trace lengths, the via size, and the via depth should be taken into account for high-speed circuit calculation. The designer should understand that the via drill size impacts the size of the via. Smaller the vias, the better will be the performance of the circuit. Once the designer decides the vias sizes, the right placement of these vias close to their respective pads should be considered.

In high-speed design, the vias are placed closed to the pad to avoid parasitic capacitance. Sometimes they are placed partially on the pad or entirely within the pad. These adjustments require DRC adjustments.

7.2.7 Component Selection and Placement

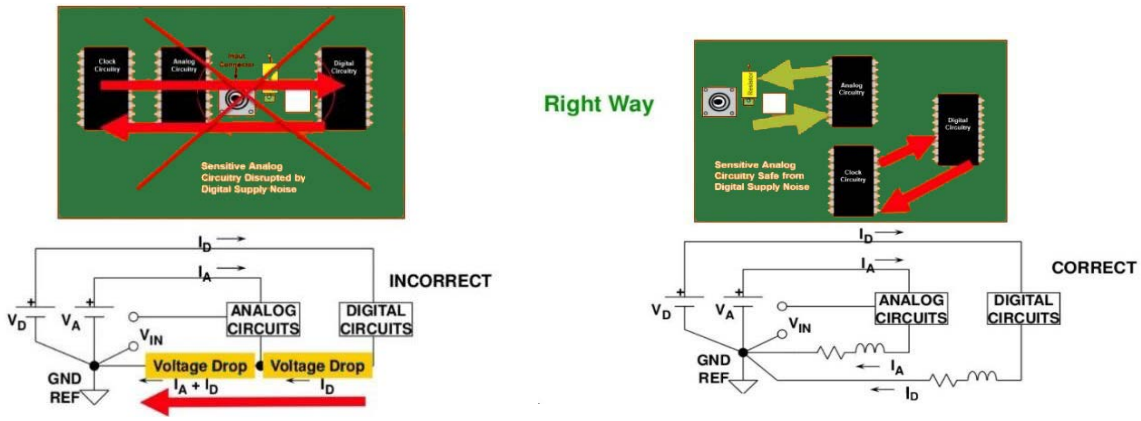
It is good practice to minimize the use of sockets since they can introduce inductance. The designer should select the correct package, and accompanying component footprint while designing for high-speed. Components like op-amps are available in different packages. One type of an op-amp may support shorter trace lengths in a circuit than the other. Finally, the component footprint shapes should be optimized for thermal considerations. The best way to dissipate heat is to place power pads right under the IC footprints that are connected to an internal plane. Even the smallest change in the pad shapes can tighten up the routing and decrease the connection lengths. This will result in a compact design.



Good Components Orientation (left) and Poor Components Orientation (right)

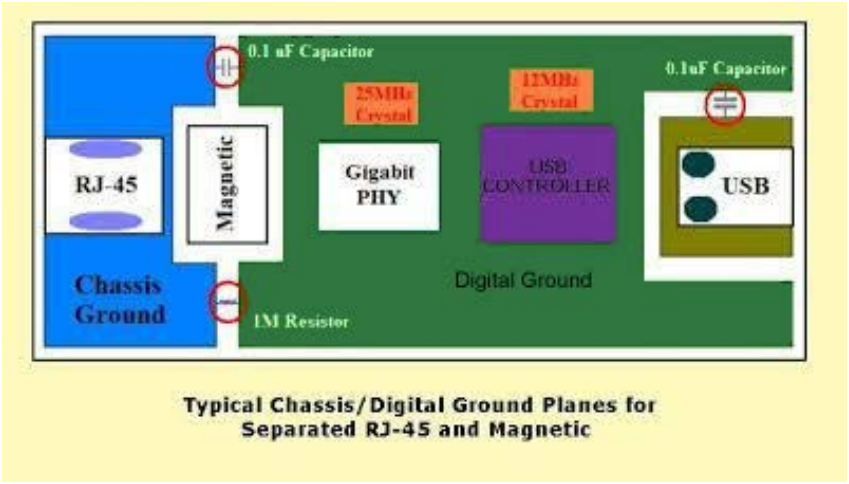
7.2.8 Separating Analog and Digital Circuits

The placement routing topologies should be implemented in a way where the analog and digital GND do not mix up. The block diagram below shows the component placement. As we can observe in the first placement scheme, the analog and digital reverse currents overlap each other. This degrades the analog signals since the reference is disturbed. The PCB designer must avoid such practices. In the second scheme, we can see the GND paths for analog and digital are isolated. Here, the digital reverse current does not interfere with the analog reference GND. The designer should adopt a placement strategy such that even if the GND is not isolated (same net), the reverse currents of either section do not interfere with each other.



7.2.9 Ground Plane Isolation

Isolate the ground planes when required in the digital section. The figure presented below shows the necessity of isolation within the digital sections. The USB and RJ45 connectors communicate externally. The board GND needs to be isolated to avoid any noise or interference from external chassis/body GND.



Typical Chassis/Digital Ground Planes for Separated RJ-45 and Magnetic

RJ45 Connector and USB Connector

7.2.10 Surge Suppressors Placement

To protect circuits from external voltage surges often surge suppressing diodes and inductors are provided in the circuits. Place these surge suppressors close to the incoming signal connectors and avoid vias connecting these surge suppressors and vias have parasitic inductances.

7.3 High-Speed Routing Strategy

In a high-speed design, a well-organized trace routing after the placement of components is necessary for a circuit to operate without any signal integrity issues. The first step in routing is stack-up design. Stack-up design is an important part of routing strategy and needs to be planned before routing traces. One of the key factors in routing controlled impedance traces is to have unbroken ground planes below and above the top and bottom layers. For inner signal layers carrying controlled impedance traces incorporate ground planes on either side of the controlled impedance traces.

The design rules are next set in the PCB design tool. The differential pair and single-ended traces are identified and the classes are defined. In the classes, the trace widths and spacings are determined. Additionally, the via sizes are also specified.

The routing is done in stages and the strategy is to route critical traces first. The designer should route crystals to the devices they are associated with first with the shortest routes. The decoupling capacitors are placed close to the power pins of the ICs and they are routed first. Also the gnd vias for the decoupling capacitors are placed. Care is taken to keep place for the trace routing. Later, the controlled impedance traces are routed. The routing is then completed.

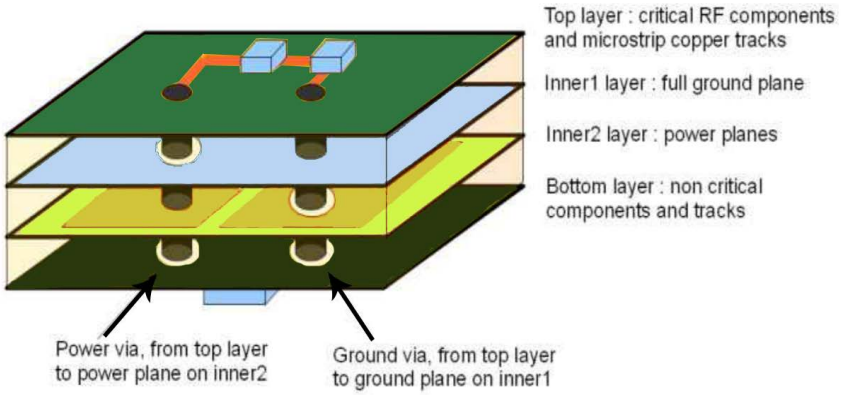
7.3.1 Best Routing Practices for High-Speed Routing

7.3.1.1 Ground and Power Planes

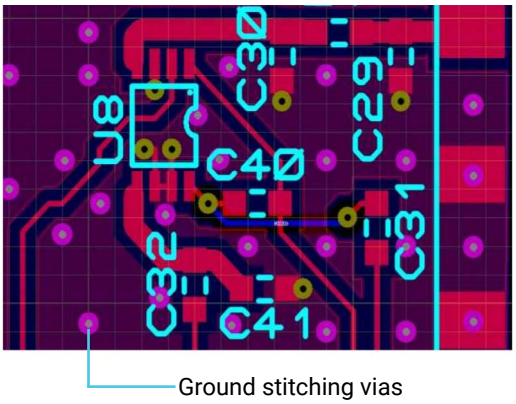
One of the most usual problems in PCB design, and also in the system design, is the lack of a good ground structure.

As a rule of thumb, it's most beneficial to have a solid-rock common ground. For best results, a designer should incorporate at least a four-layer PCB. A four-layer PCB allows devoting one of the inner layers to a full ground plane. A ground plane composed of a full, plain, sheet of copper, as large as the PCB, ensures minimal impedance between any couple of grounded points. This ground plane should never be broken by routing any small track in it. There should exist only one ground plane on that layer.

When some of the copper is removed on this ground plane, parasitic impedances are introduced immediately on the neighboring tracks. In this kind of a design, usually, the side nearest to the ground plane is used to mount all the high-speed components like RF components using microstrip techniques. The opposite side is used for mounting less critical components. The second inner layer is used for power distribution and different power islands are placed in this layer such as 3.3V, 1.8V, 5V, etc. The power islands are made as large as possible in order to reduce the impedance.



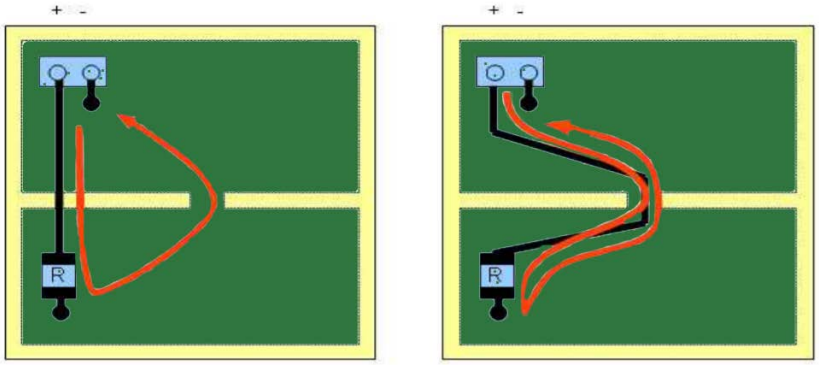
A double-sided PCB may be the right choice for economical use when it comes to cost minimization. Achieving this is quite difficult. When there is a requirement to route tracks on both sides of the PCB in the same area then a good ground plane is no longer guaranteed. The only solution is then to implement huge ground planes on both sides that are interconnected by plenty of vias.



Designing a double-sided PCB can get complex since the ground plane gets shared between the top and bottom layers. The designer should ensure that there is at least a full ground plane under the most critical section. The top side must be used for routing as much as possible with a few traces on the bottom side.

Lots of interconnecting vias are needed to interconnect the top and the bottom grounds.

Split ground planes are sometimes implemented in critical cases. For instance, a ground plane for the logic sections and a ground plane for the analog components, interconnected at a single point. The concept is to reduce the noise through the ground planes. Sadly, it is quite challenging to accurately implement such an idea. In particular, it is then mandatory to route all the traces going from one region to the other exclusively above this interconnecting point. If not then this gives a very good antenna which will either transmit or receive spurious signals. In most cases, a full single ground is more reliable and provides better results than split grounds, as long as the placement of the components is adequate.



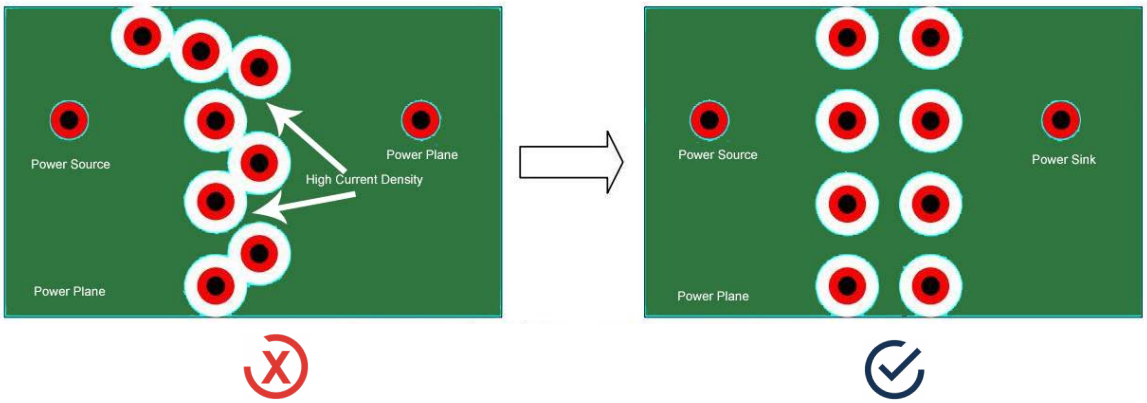
Large current loop area :
Strong radiated field

Small current loop area :
Low radiated field

Usually, a split ground plane is avoided unless there is a specific need like strong ESD risks. Or else, any track going from one ground area to the other should cross the boundary just under the interconnecting point. If not, then there will be a current loop leading to EMC problems.

7.3.1.2 Polygon Voids

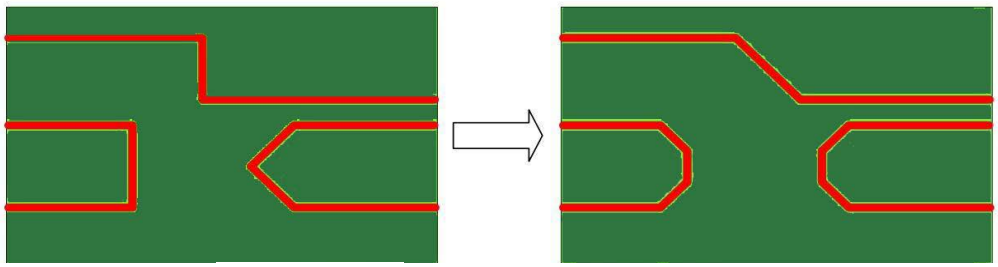
The signal vias produce voids in the power and ground planes. Improper positioning of vias can create plane areas in which the current density is increased. These regions are called hot spots. These hot spots must be avoided. The best solution is to place the vias such that there is enough space between the vias for the power plane to pass through. As a thumb rule, place vias 15 mils apart wherever possible.



Avoid copper plane hot spots.

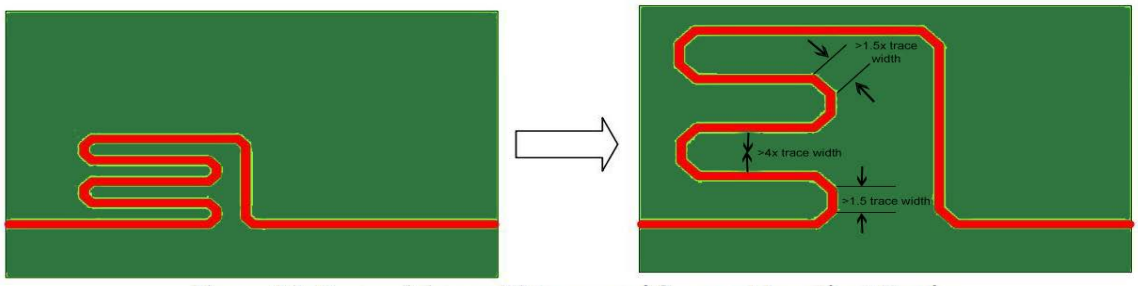
7.3.1.3 Trace Bend Geometry

The bends should be kept minimum while routing high-speed signals. If the bends are required, then 135° bends should be implemented instead of 90°.



Use 135º bends instead of 90º.

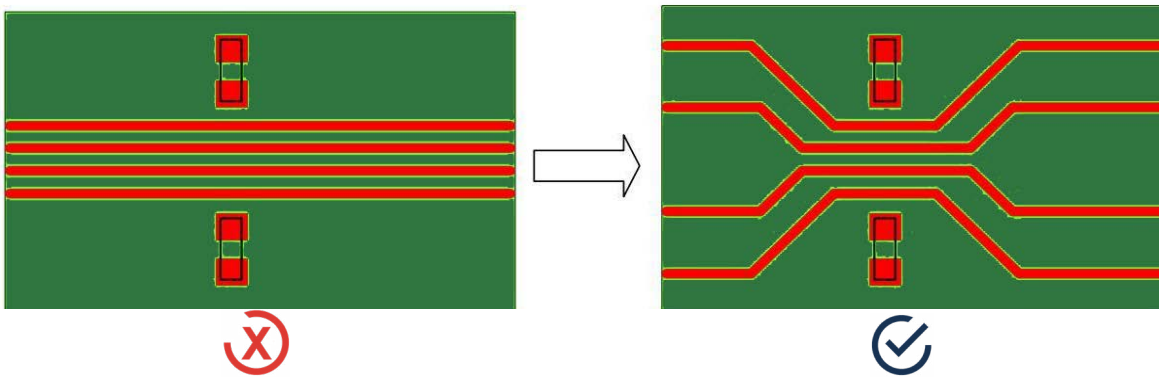
To achieve a specific trace length, serpentine traces are needed. A minimum distance of 4 times the trace width must be maintained between adjacent copper in a single trace. Each segment of the bends should be 1.5 times the trace width. Most of the DRCs in CAD tools do not check these minimum distances as the traces are part of the same net.



Keep minimum distance and segment length at bends.

7.3.1.4 Signal Proximity

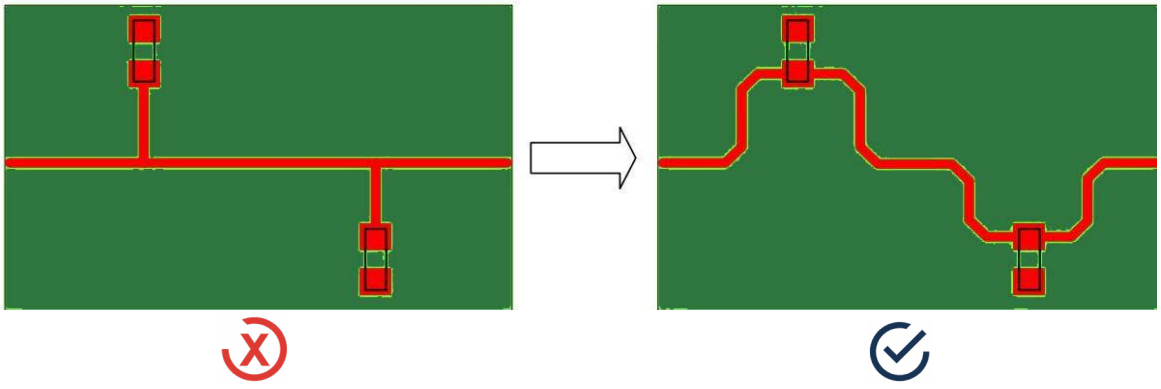
A minimum distance should be maintained between traces to minimize the crosstalk. The crosstalk level depends on the length and the distance between two traces. In some areas, the routing of traces reaches a bottleneck where the traces are closer than the allowed distance between them. In such situations, the distance between the signals outside the bottleneck should be increased. Even if the minimum requirement is met, the spacing can be increased a little further.



Increase the spacing between traces wherever possible.

Trace stubs:

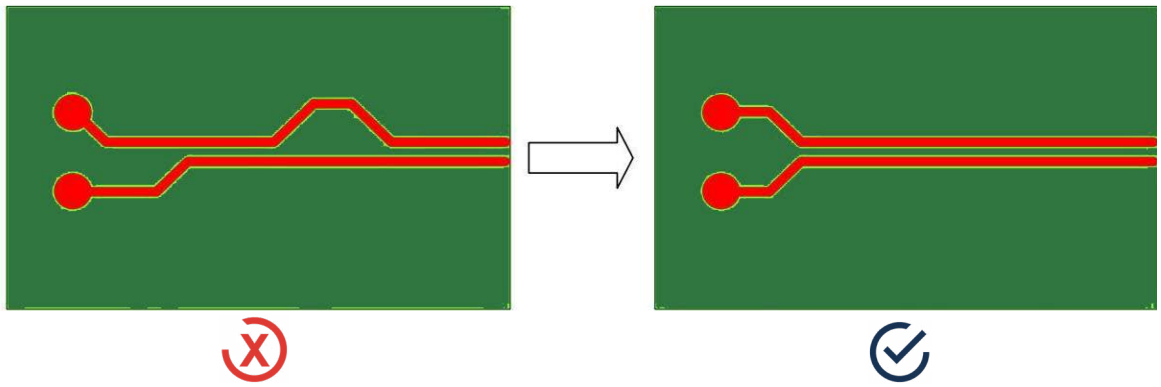
The long stub traces may act as antennas and consequently increase problems complying with EMC standards. Stub traces can also create reflections that negatively affect signal integrity. Pull-up or pull-down resistors on high-speed signals are common sources of stubs. If such resistors are required then route the signals as a daisy chain.



Avoid stub traces by implementing daisy chain routing.

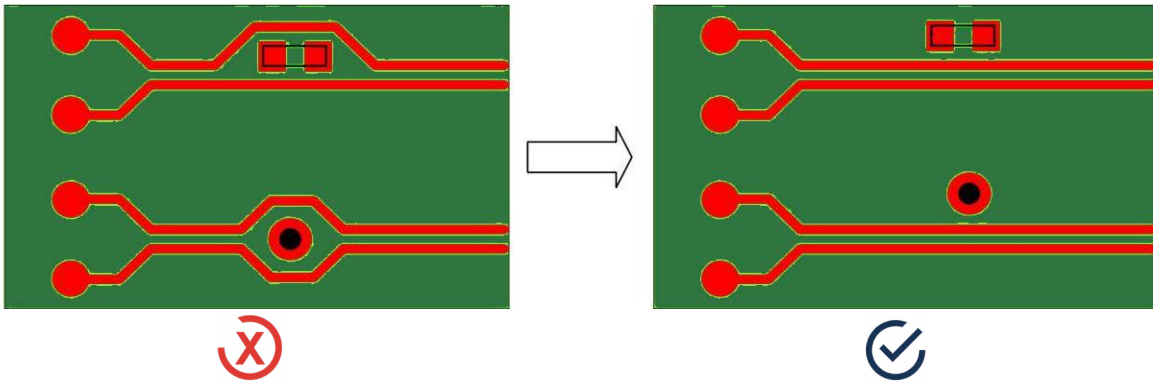
7.3.1.5 Differential Pair Signals

When routing high-speed differential pairs parallel to each other, a constant distance should be maintained between them. This distance helps to achieve the specified differential impedance. The designer should minimize the area in which the specified spacing is enlarged due to pad entries. The differential pairs should be routed symmetrically.



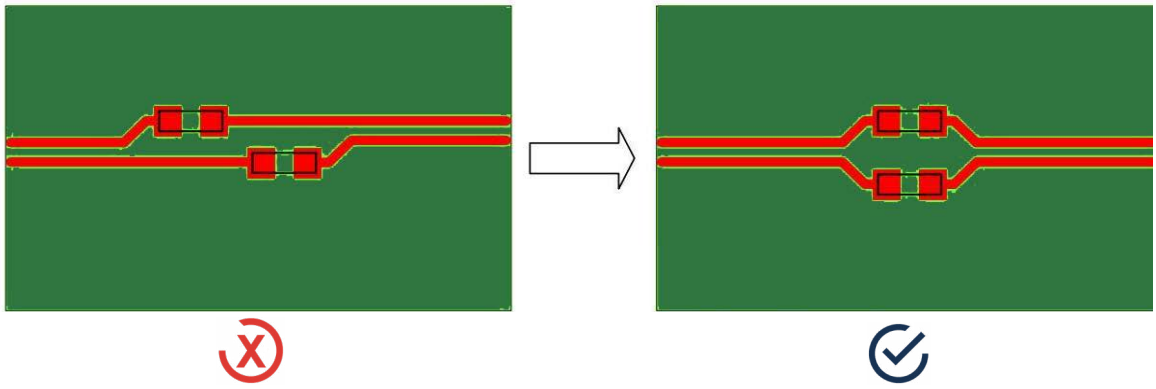
Route the differential pairs symmetrically and keep the signals parallel.

The designer should not place any components or vias between differential pairs even if the signals are routed symmetrically. Placement of components and vias between differential pairs could lead to EMC problems and impedance discontinuities.



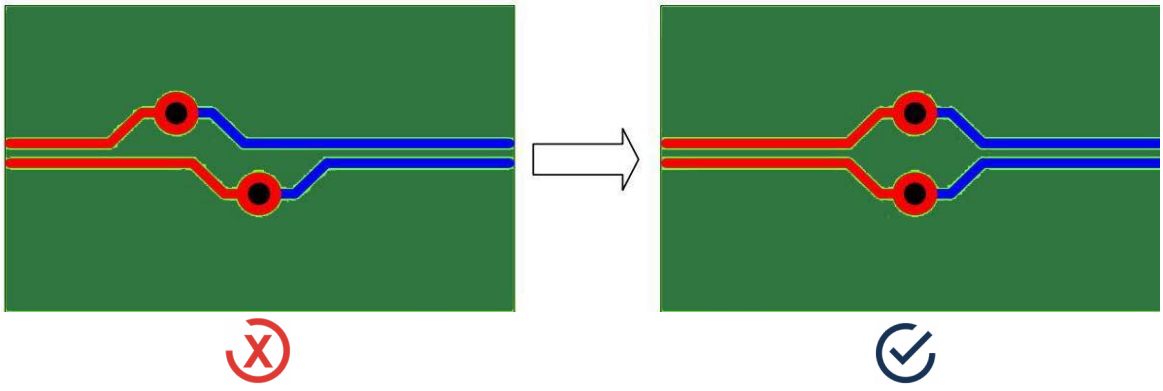
Do not include any components or vias in-between a differential.

Some high-speed differential pairs need serial coupling capacitors. These capacitors should be placed symmetrically. The capacitors and the pads produce impedance discontinuities. Capacitor sizes such as 0402 are preferable, 0603 are acceptable. Larger packages such as 0805 or C-packs must be avoided.



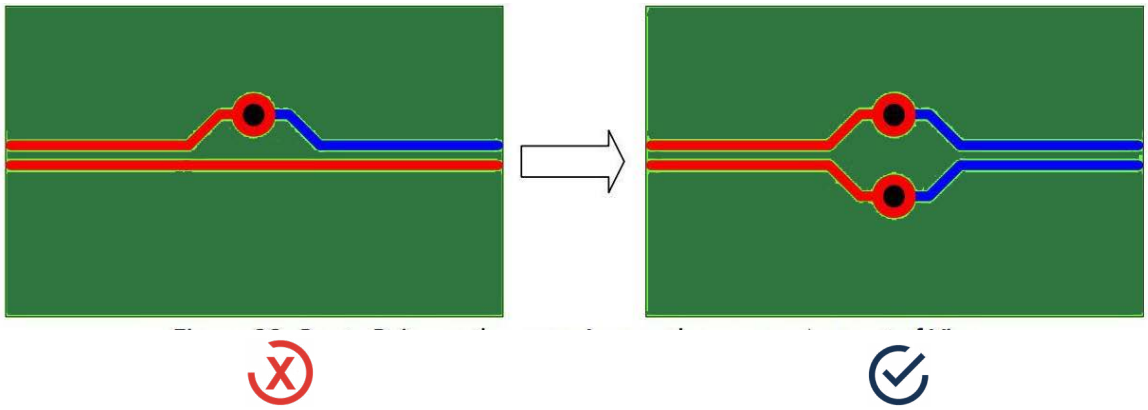
Place coupling capacitors symmetrically

Since the vias introduce an enormous discontinuity in impedance, the number of vias must be reduced and should be placed symmetrically. If the signals change the planes then the ground transition vias are required.



Place vias symmetrically.

While routing a differential pair, both the traces should be routed on the same layer so that the impedance requirements are met. Also, the same number of vias should be included in the traces.

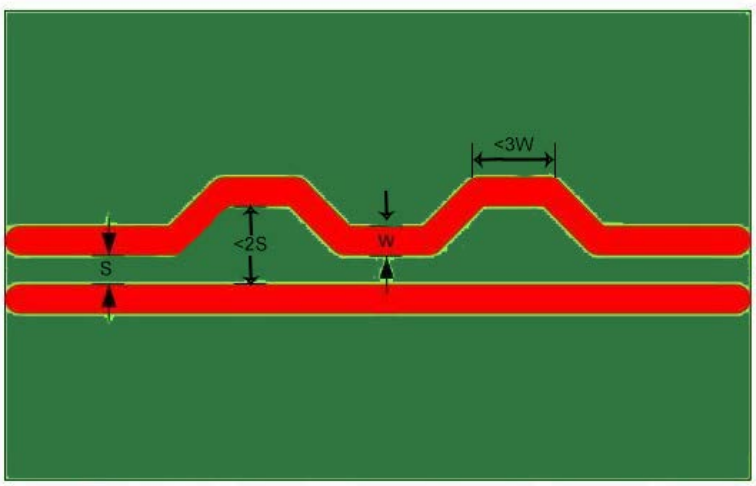


Route pairs on the same layer and place the same number of vias.

7.3.1.6 Length Matching

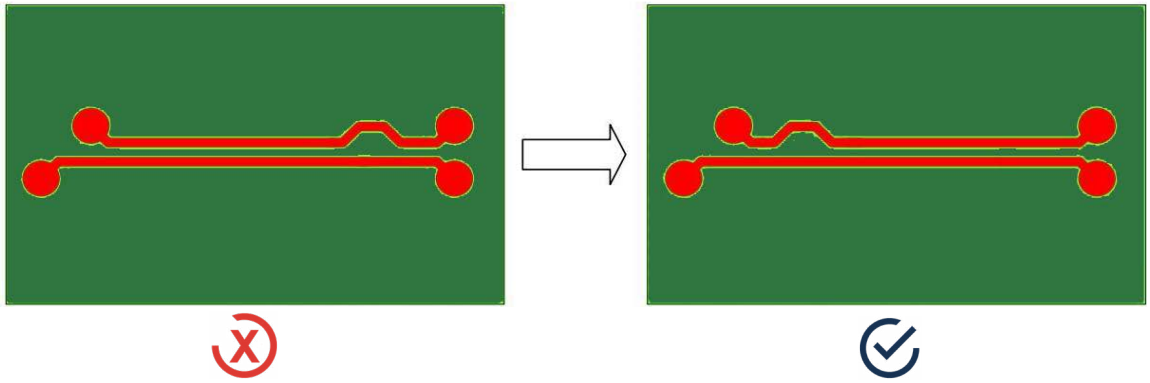
The high-speed interfaces have additional requirements concerning the time of arrival clock skew between different traces and pairs of signals. For instance, in a high-speed parallel bus, all data signals need to arrive within a time period in order to meet the setup and hold time requirements of the receiver. The PCB designer should ensure that such permitted skew is not exceeded. To achieve this requirement, the length matching is necessary.

The differential pair signals demand a very tight delay skew between the positive and negative signal traces. Hence, any length differences should be compensated by using serpentines. The geometry of serpentine traces should be carefully designed in order to reduce impedance discontinuity.



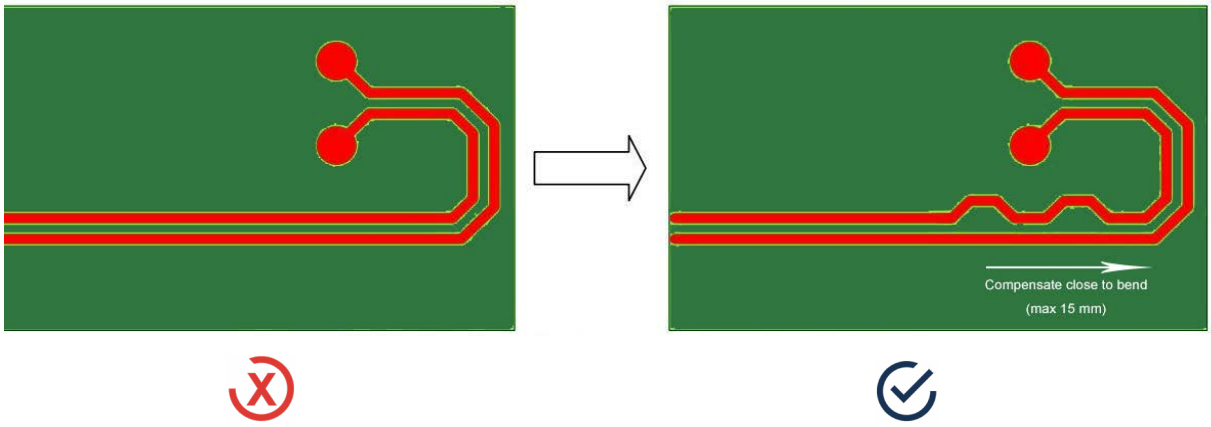
Use this recommended serpentine trace geometry.

The designer should place the serpentine traces at the root of the length mismatching. This ensures that the positive and negative signal components are propagated synchronously over the connection.



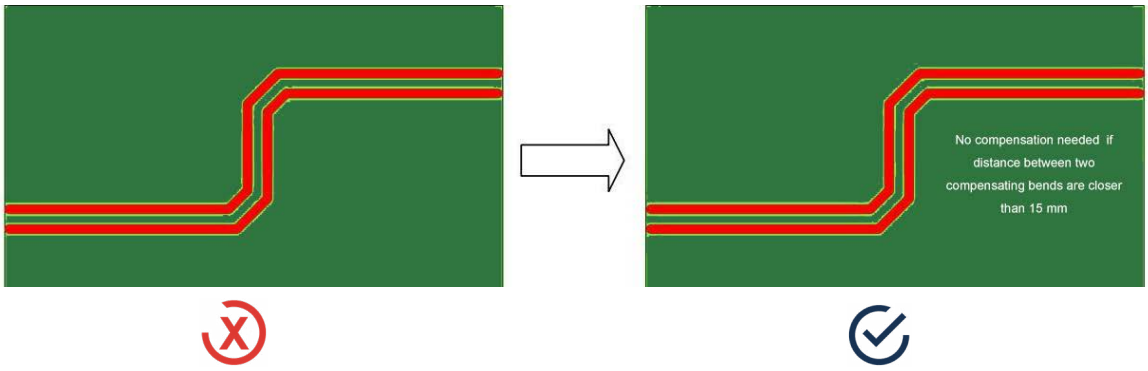
Add length correction to the mismatching point.

The bends are usually the source of length mismatches. The compensation should be planted very close to the bend with a maximum distance of 15mm.



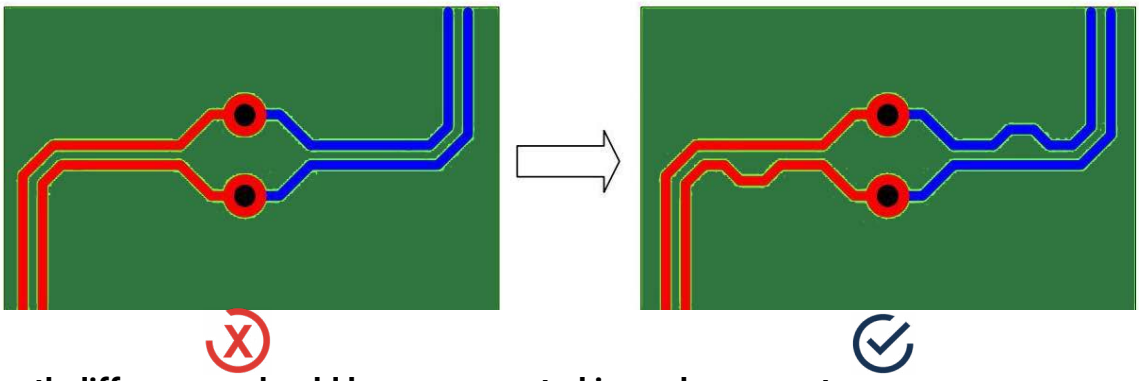
Place length compensation close to the bends.

Generally, two bends compensate each other. If the bends are closer than 15mm then no additional compensation with serpentines are necessary. The signals should not traverse asynchronously over a distance more than 15mm.



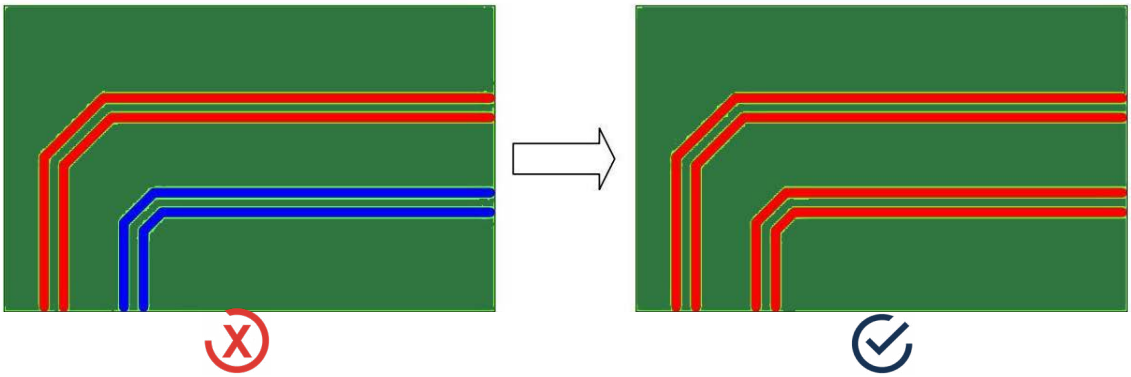
Bends can compensate each other.

The mismatches in each segment of a differential pair connection should be matched individually. In the figure shown below, the vias separate the differential pair into two segments. The bends need to be compensated individually here. This ensures that the positive and negative signals are propagated synchronously through the vias. The DRC overlooks this violation since it only checks the length difference over the whole connection.



Length differences should be compensated in each segment.

The signal speed is not the same in all the layers of a PCB. Since it is hard to figure out the difference, it is preferable to route signals on the same layer if they need to be matched.

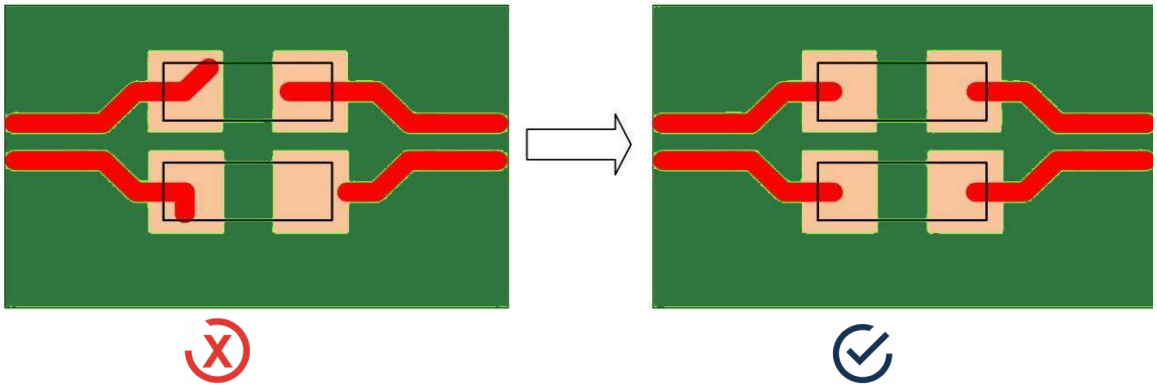


Pairs within the same interface should be preferably routed on the same layer.

Some of the CAD tools also consider the trace length inside a pad to its total length. The figure shown below depicts two layouts which are similar from an electrical point of view.

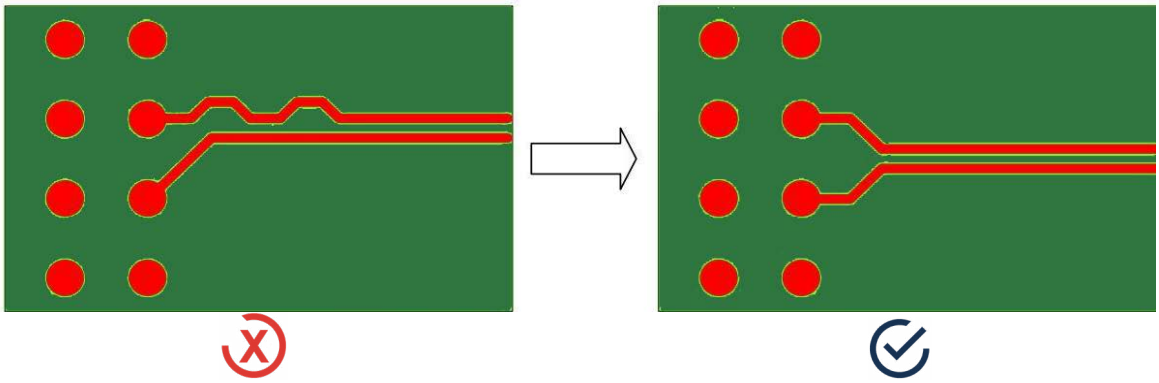
In the left figure, the traces inside the capacitor pads do not have an equal length. Even though the signals are not using the internal traces, some CAD tools consider this as part of the length calculation and display a length difference between the positive and negative signals. In order to minimize this, ensure that the pad entry is equal for both signals.

In the same way, some CAD tools do not consider the length of vias when calculating the total length. Since differential pairs should have the same amount of vias in both traces, the error does not affect the length matching. However, it can affect calculations for matching two differential pairs or the matching of parallel buses.



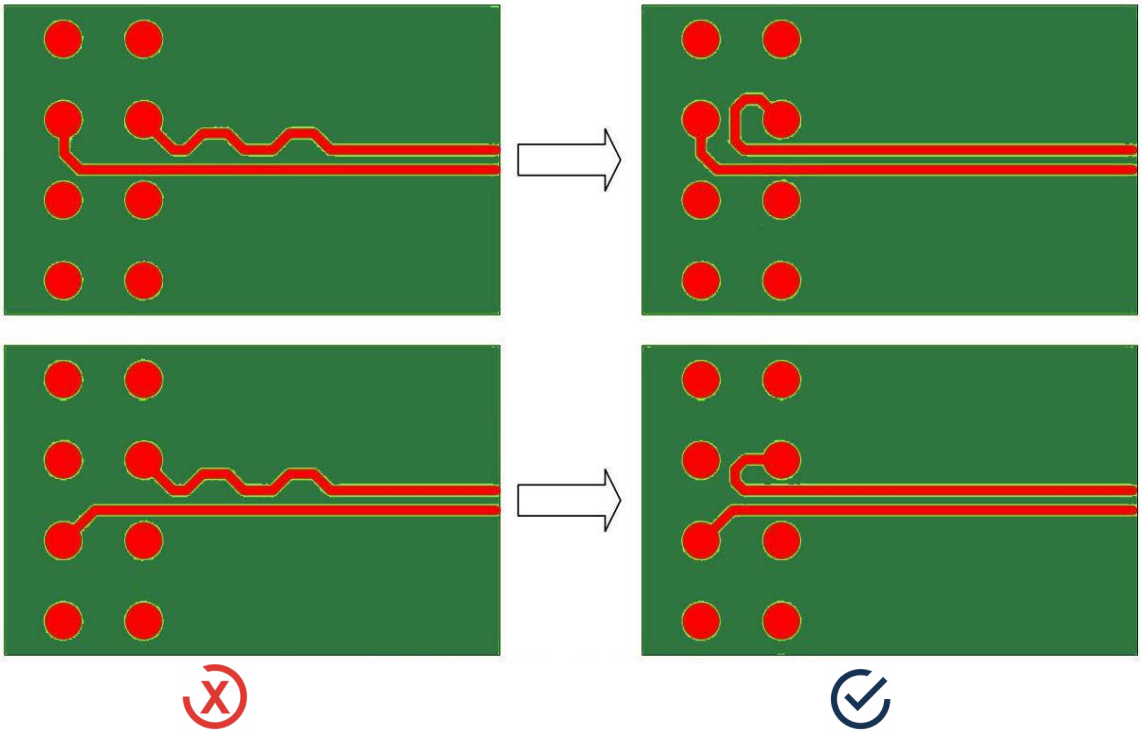
Pay attention to length calculation issues encountered in some CAD tools.

A symmetric breakout of differential pair signal is preferred wherever possible in order to avoid the serpentine traces.



This is the preferred symmetrical breakout.

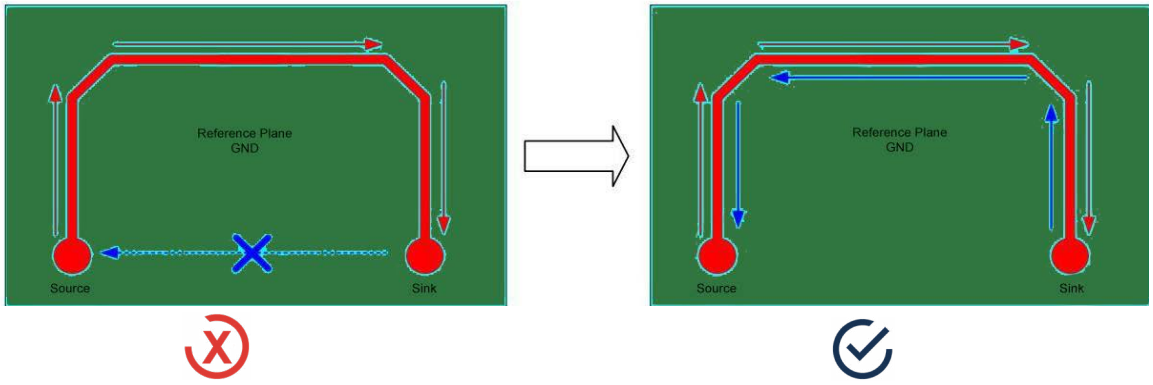
Small loops can be included for the shorter trace instead of serpentine traces if there is enough space between pads. This is generally preferred over a serpentine trace.



This is the preferred breakout of differential pairs.

7.3.1.7 Signal Return Path

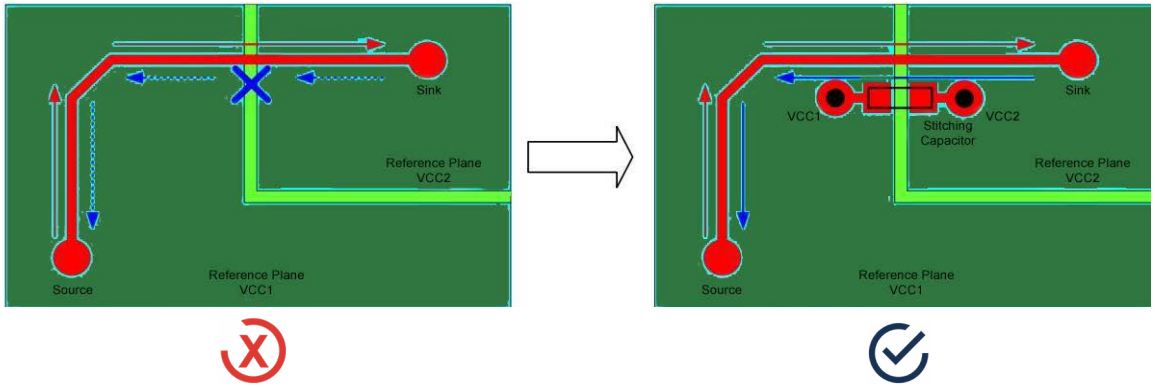
An incorrect signal return path results in noise coupling and EMI issues. The designer should always think of the signal return path when routing a signal. The power rails and low-speed signals take the shortest return current path. In contrast to this, the return current of high-speed signals tries to follow the signal path.



In high-speed signals, the return current tries to follow the signal path.

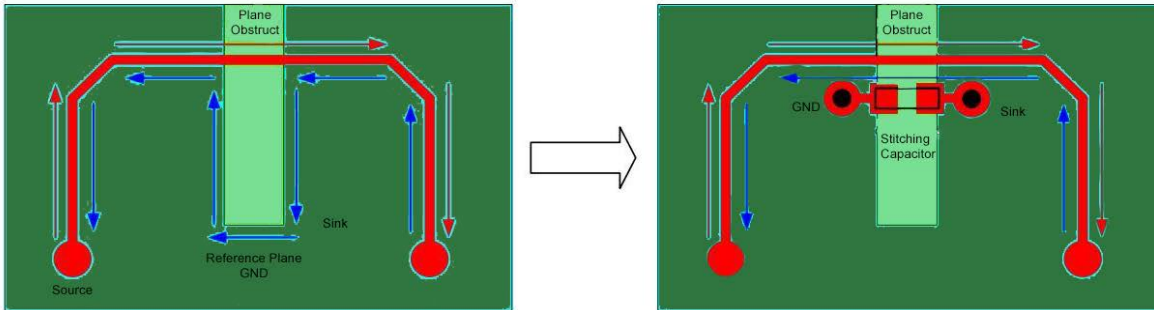
A signal should not be routed over a spit plane as the return path is not able to follow the signal trace. If a plane is split between a sink and source, route the signal trace around it. If the forward and return paths of a signal are separated, the area between them acts as a loop antenna.

Stitching capacitors should be incorporated if a signal needs to be routed over two different reference planes. The stitching capacitor enables the return current to travel from one reference plane to the other. The capacitor should be placed close to the signal path so that the distance between the forward and return path are kept small. Generally, the values of stitching capacitors are between 10nF and 100nF.



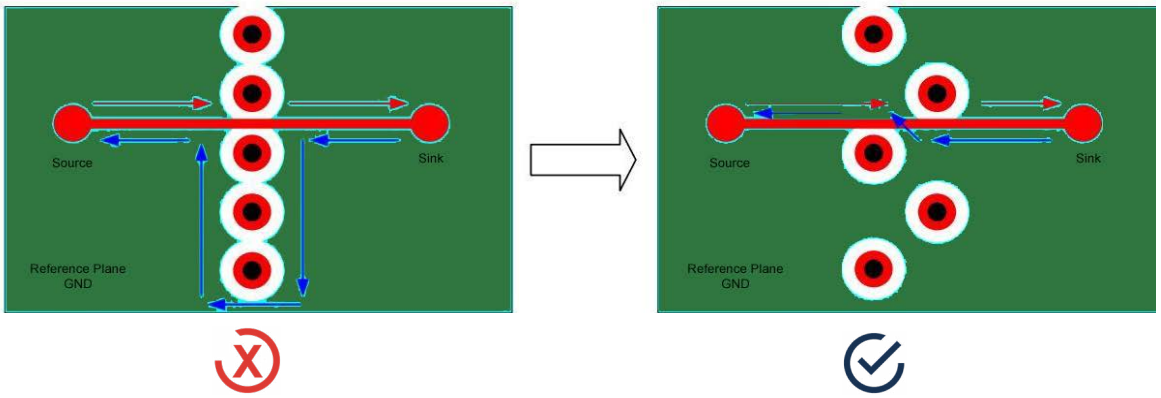
Placement of stitching capacitors over split planes.

In general, plane obstructions and plane slots must be avoided. If it is really necessary to route over such obstruction then stitching capacitors should be used.



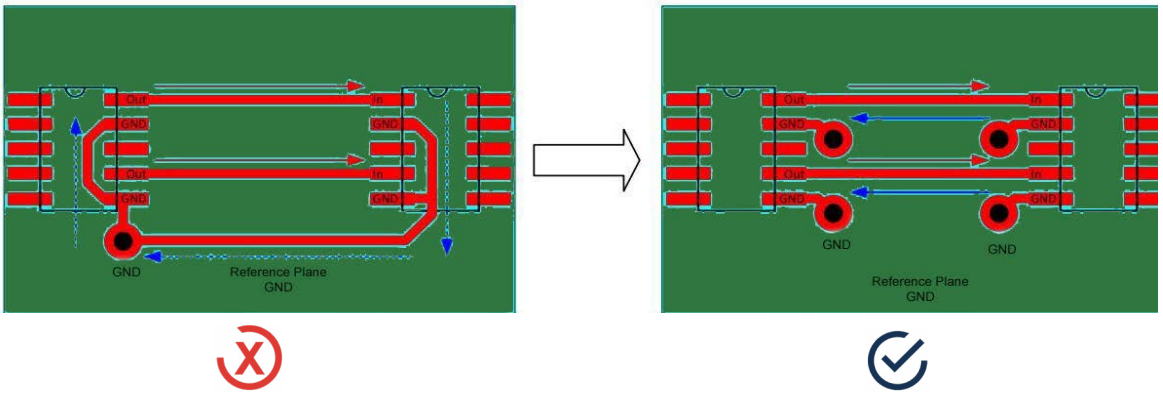
Stitching capacitors incorporated when routing over plane obstructs.

The designer should look out for voids in reference planes while routing high-speed signals. Voids in reference planes are generated when placing vias close together. Large void areas should be avoided by ensuring adequate separation between vias. It is better to place fewer ground and power vias in order to reduce via voids.



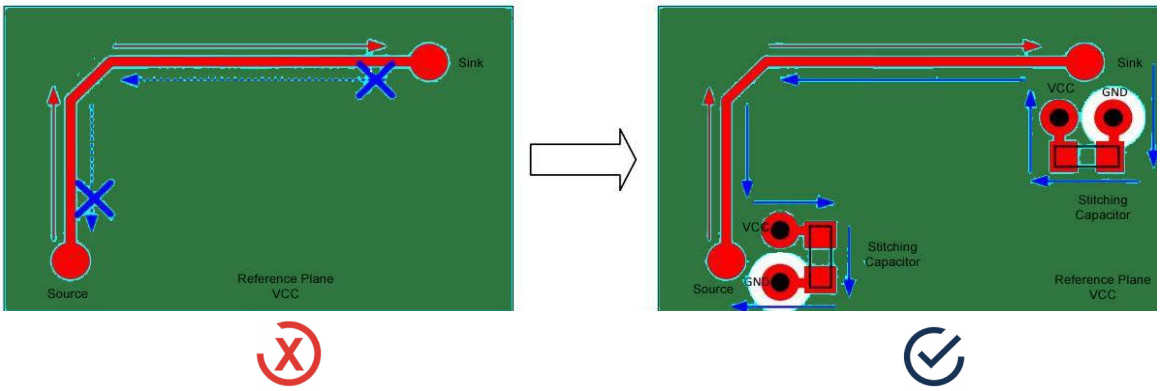
Avoid via plane voids.

The return path should be considered at the source and sink of a signal. In the figure shown below, the left design is considered to be a bad design. Since there is only one single ground via on the source side, the return current cannot travel back over the reference ground plane as intended. The return path is the ground connection present on the top layer instead. The problem in hand is that the impedance of the signal trace is calculated as referenced to the ground plane and not to the ground trace on the top layer. Hence, it is essential to place ground vias at the source and sink side of the signal. This allows the return current to travel back on the ground plane.



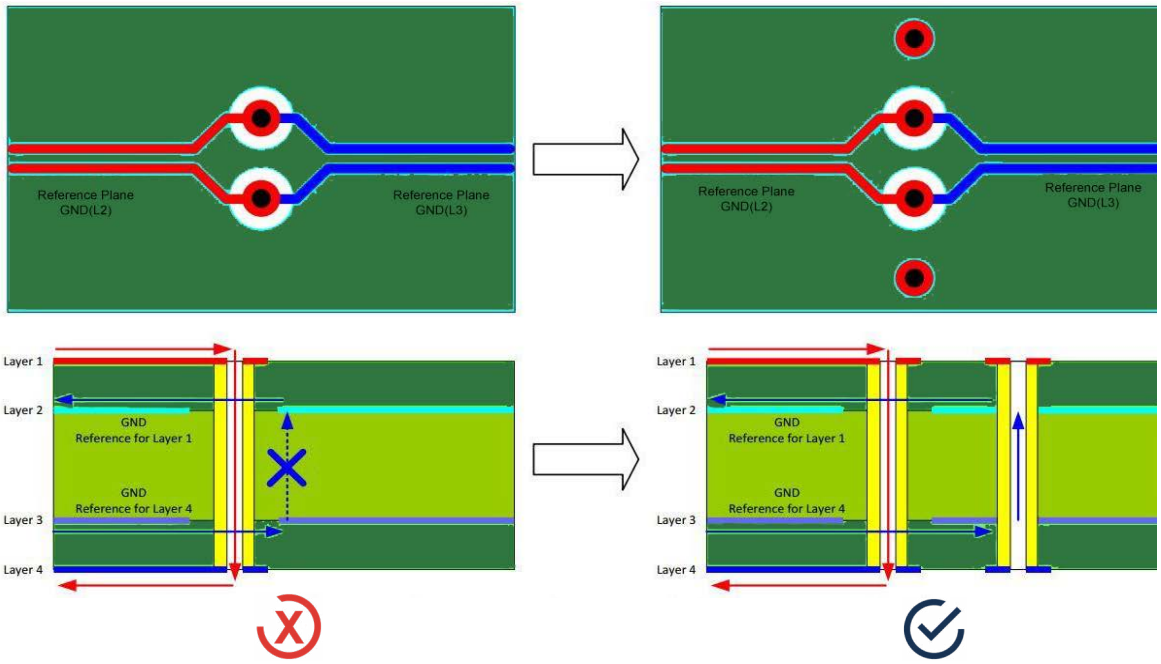
Return path should be considered when placing ground vias.

As far as possible avoid using power planes as references. But when a power plane is considered as a reference to a signal, then the signal should be able to propagate back over the power plane. The signals are referenced to ground in the source and sink. To switch the reference to the power plane, stitching capacitors should be incorporated at the sink and source. If the sink and source are utilizing the same power rail for their supply, then the bypass capacitors can act as stitching capacitors if they are placed close to the signal entry/exit point. The ideal value for the stitching capacitor is between 10nF and 100nF.



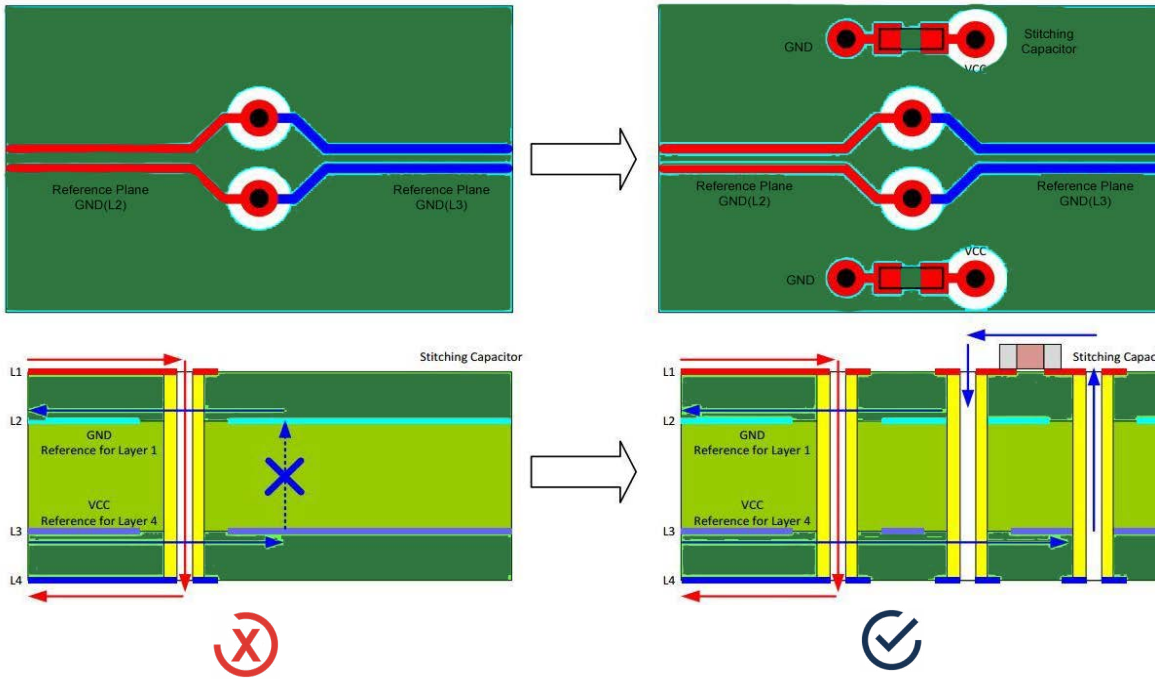
Include stitching capacitors when using power planes as reference.

When a signal switches a layer, the reference ground plane will also be switched. Hence, stitching vias should be added close to the layer change vias. This permits the return current to change the ground plane. When dealing with differential signals, the switching ground vias should be placed symmetrically.



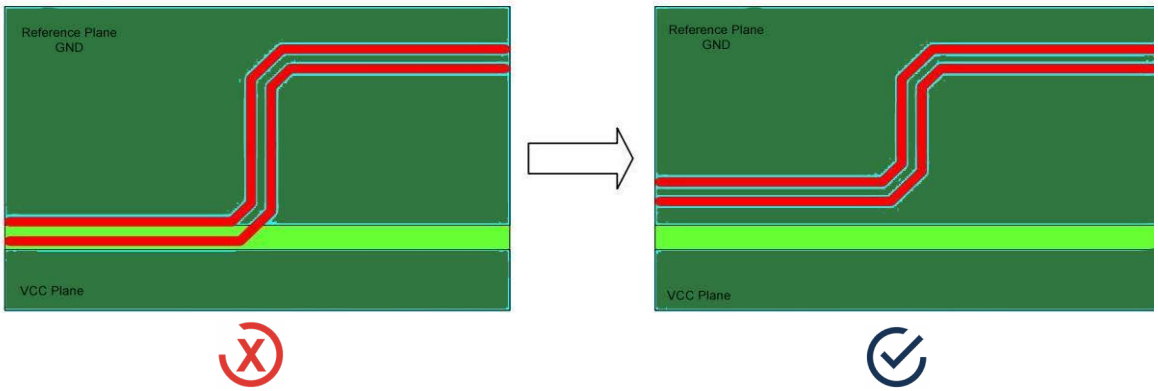
Stitching capacitors should be included when signal changes ground reference.

When a signal switches to a layer that has a different net as a reference then stitching capacitors should be implemented. This permits the return current to flow from the ground to the power plane through the stitching capacitor. Also, the stitching capacitor placement and routing should be symmetrical when differential pairs are considered.



Incorporate stitching capacitors when signal reference plane changes.

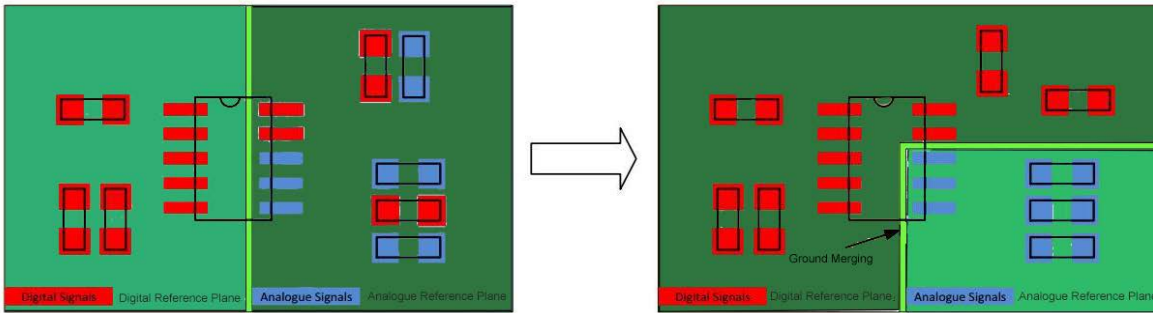
The designer should not route high-speed signals on the edge of the reference planes or close to PCB borders. This can have an adverse impact on the trace impedance.



High-speed signals should not be routed at plane and PCB edges.

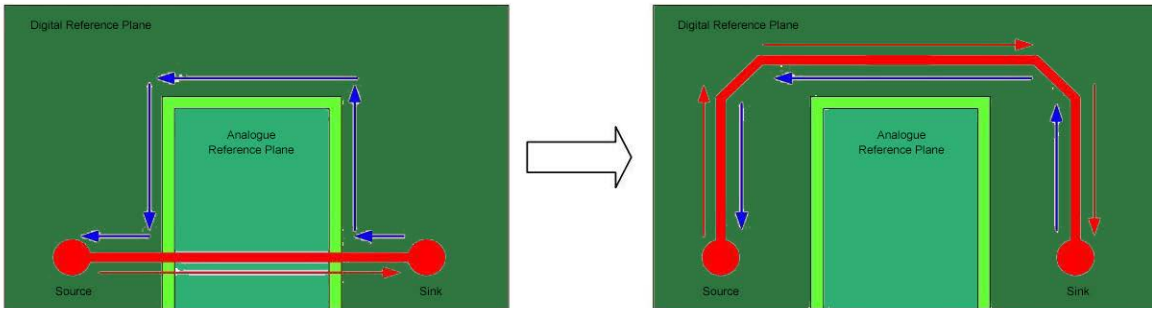
7.3.1.8 Split Plane Approach

The split ground approach makes it easy in the schematic to determine which components and pins should be connected to the digital ground and which ones to the analog ground. These kinds of schematics can be routed by placing two different ground planes as reference. The two planes should be placed accurately. The analog ground must be placed underneath the analog pins and components. Note: It is always preferable to have one solid ground plane.



Power plane splitting needs to be placed carefully.

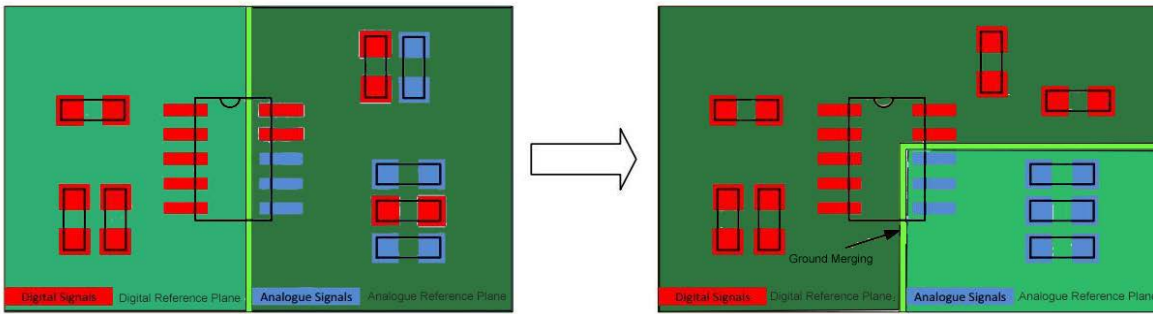
The mixed-signal circuits require the analog and digital ground connected together at a single point. In the reference schematics, it is always recommended to place ferrite beads or zero-ohm resistors between the two nets. The merging of the digital and analog ground should be placed close to the integrated circuit. In a mixed-signal design that has split planes, the digital signal should not be routed over an analog ground plane and the analog signal should not be routed over the digital ground plane.



Digital signals should not cross the analog ground plane.

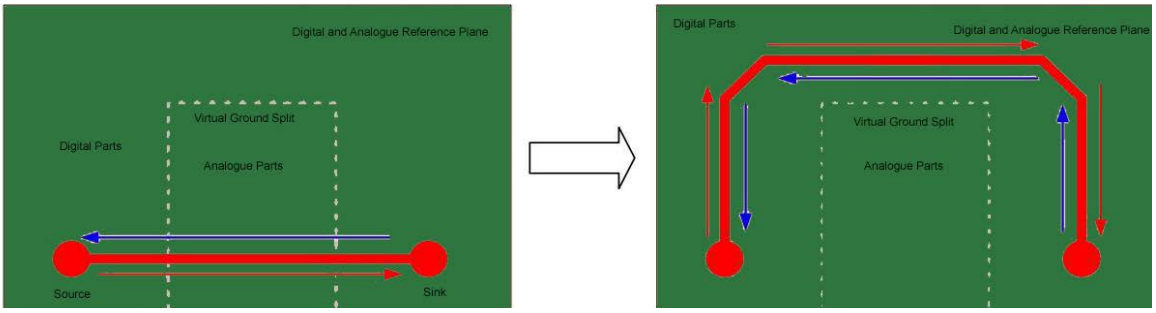
7.3.1.9 Virtual Split Approach

In the virtual split approach, the analog and digital ground are not separated in the schematic diagram. Also, in the two ground domains are not electrically split in the layout either. Interestingly, the layout is split virtually, i.e., an imaginary separation is drawn between the analog and digital ground. The components should be placed carefully considering the correct side of the virtually split planes.



Components should be placed carefully with virtual plane splitting.

The designer should keep in mind the virtual line between the two ground domains during the routing process. Neither the digital nor the analog signal trace is allowed to cross the virtual split line.

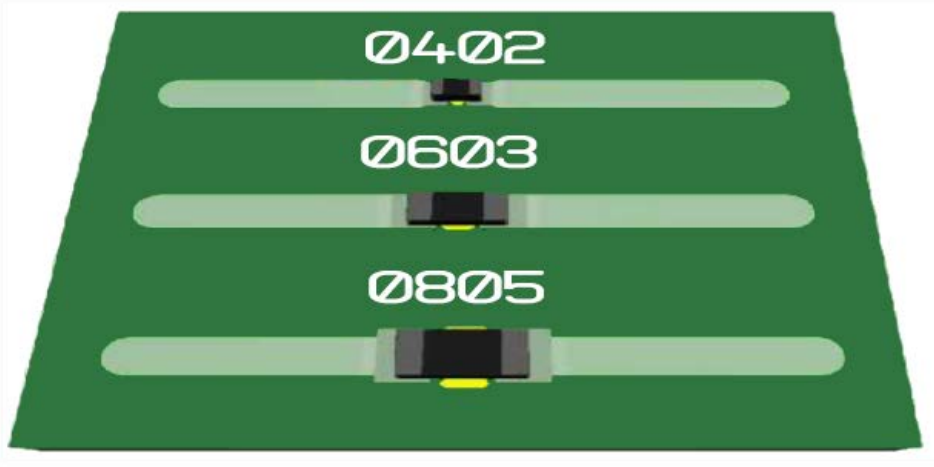


Digital signals should not cross the virtual analog ground.

7.3.1.10 Components Selection for High Speed Design

The board design begins with the schematic, specifically with the selection of the components. The surface-mount devices (SMD) are preferred since smaller components and shorter wires result in stablest high-speed performances.

Choosing the package can get tricky sometimes. One beneficial criterion is to look at the track width calculated for a 50-ohm impedance. The best high-speed performances are usually accomplished if the width of the component is close to track width. This will lower the impedance matching issues between the track and the component pad.



The impedance mismatches can be reduced by selecting those components that have a package that is almost the same size as of the calculated track width. The test points should be planned at the schematic phase.

TIP:

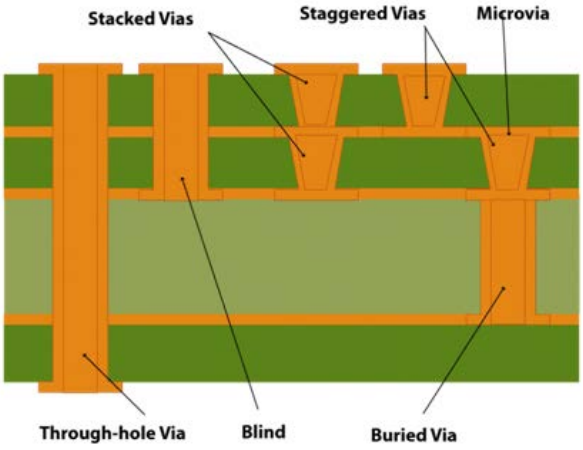
When it comes to power supplies, implement separated digital and analog power supplies, even using only a small SMT ferrite bead to isolate them. If there are successive high frequency amplifying stages, then decouple the power supply of these successive circuits, or else this might result in an oscillation somewhere in the circuit.

7.4 Vias and Microvias

In a high-speed circuit, any mental on the PCB should be considered as part of that circuit. The trace lengths, the via size, and the via depth should be taken into account for high-speed circuit calculation. The designer should understand that the via drill size impacts the size of the via. Smaller the vias, the better will be the performance of the circuit. Once the designer decides the vias sizes, the right placement of these vias close to their respective pads should be considered.

In high-speed design, the vias are placed closed to the pad to avoid parasitic capacitance. Sometimes they are placed partially on the pad or entirely within the pad. These adjustments require DRC adjustments.

7.4.1 Different Types of Vias



Depending on their functionality, there are different types of vias that are drilled into a PCB.

7.4.1.1 Through-hole Vias

The hole penetrates from the top layer to the bottom layer. They can be either PTH or NPTH. For PTH, the connection is established from the top to the bottom layer.

7.4.1.2 Blind Vias

The hole penetrates from an exterior layer and ends at an interior layer. Here, the hole doesn't penetrate through the entire board but connects the PCB's exterior layers to at least one interior layer. Either the connection is from the top layer to a layer in the center or from the bottom layer to some layer in the interior region. The other end of the hole cannot be seen once the lamination is done. Hence, they are called blind vias.

7.4.1.3 Buried Vias

These vias are located in the interior region of the PCB. The buried vias have no paths to the outer layers. They connect the inner layers and stay hidden from sight. As per IPC standards, buried vias and blind vias must be 6 mils (150 micrometers) in diameter or less.

7.4.1.4 Microvias

The most commonly known vias are the microvias (μvias). During PCB manufacturing, microvias are drilled by lasers and have a smaller diameter compared to the standard through-hole vias. Microvias are generally implemented in High-Density Interconnection (HDI) PCBs. The depth of a microvia isn't usually more than two layers deep since the plating of copper inside these small vias is a tedious task. The smaller the diameter of a via, the higher should be the throwing power of the plating bath to achieve electroless copper plating.

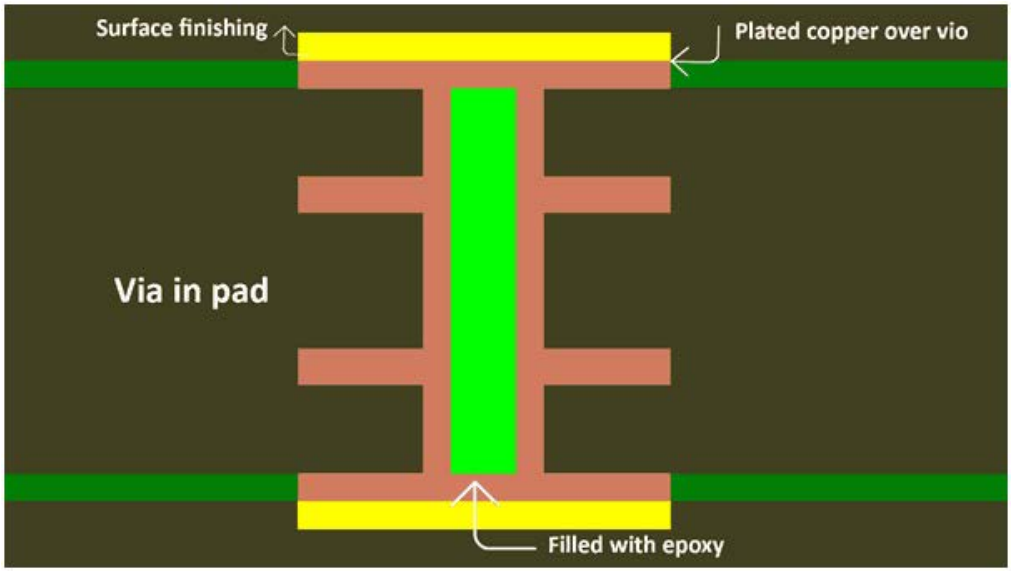
Microvias can be classified into stacked vias and staggered vias based on their location in the PCB layers.

- Stacked vias are piled on top of one another in different layers.
- Staggered vias are scattered in the different layers. And they are more expensive.
- Additionally, there is another type of microvias called skipvias. Skipvias skip one layer, meaning, they pass through a layer making no electrical contact with that specific layer. The skipped layer will not form an electric connection with that via.

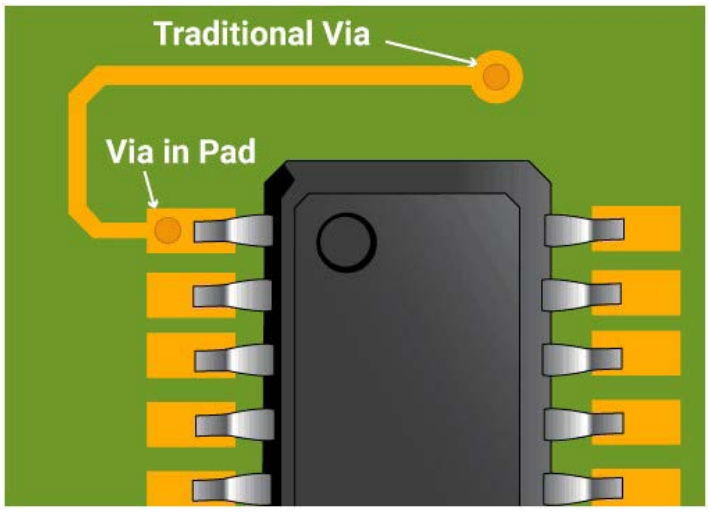
Microvias improve the electrical characteristics and also allow miniaturization for higher functionality in less space. This, in turn, makes room for large pin-count chips that can be found in smartphones and other mobile devices.

Microvias reduce the layer count in printed circuit board designs and enable higher routing density. This eliminates the need for through-hole vias. The microvias micro size and capabilities have successively increased processing power. The implementation of microvias instead of through-holes can reduce the layer count of PCBs and also ease the BGA breakout. Without microvias, you would still be using a big fat cordless phone instead of your sleek little smartphone.

7.4.1.5 Via-In-Pad



Implementation of via in pad or via in pad plated over (VIPPO) in your design

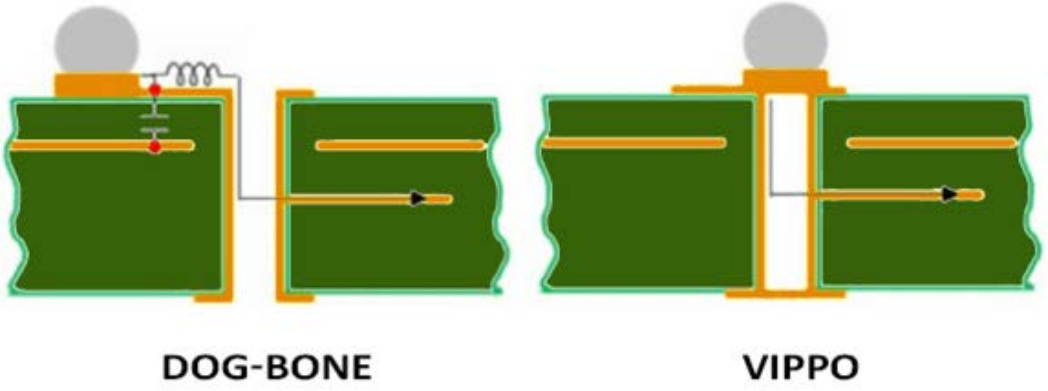


Via-In-Pad Vs. Traditional Via

The increasing signal speed, board component density, and PCB thickness have led to the implementation of via-in-pad. The PCB design (CAD design) engineers implement VIPPO along with the conventional via structures in order to achieve routability and signal integrity requirements.

7.4.1.5.1 What is Via-in-pad?

In traditional vias, the signal trace is routed away from the pad and then to the via. You can see this in the above diagram. This is done to avoid seepage of the solder paste into the via during the reflow process. In a via-in-pad, the drilled via is present right below a pad. To be precise, the via is placed within the pad of a surface mount component.



Traditional dog bone and VIPPO

First, the via is filled with non-conductive epoxy depending on the designer's requirement. Later, this via is capped and plated to regain the land area. This technique shrinks the signal path lengths and as a result eliminates the parasitic inductance and capacitance effect.

The via-in-pad accommodates smaller component pitch sizes and shrinks the PCB's overall size. This technology is ideal for BGA footprint components.

To make things better, back-drilling process is implemented along with the via-in-pad. The back drilling is performed to eliminate the signal reflections within the unused portion of the via. The unwanted via stub is drilled to remove any kind of signal reflection. This ensures signal integrity.

7.4.2 PCB Design Tips for Vias

Here are a few quick tips that you can consider while employing vias in your design:

- Use maximum micro via structures in your design.
- Stacked and staggered vias: Choose staggered instead of stacked vias since the stacked vias need to be filled and planarized. This process is time consuming and expensive as well.
- Keep the aspect ratio minimum. This provides better electrical performance and signal integrity. Lower noise and crosstalk, and lower EMI/RFI.
- Implement smaller vias. This can help you build an efficient HDI PCB since the stray capacitance and inductance gets reduced.
- Via-in-pads must be filled, unless they reside in thermal pads.
- The pad matrix on which a BGA will be installed may include through vias and blind vias, but all of them must be filled and planarized, otherwise solder joints will be compromised.
-

- Incorporate vias in the thermal pads under QFNs to help solder flow through to conductive planes.
- The vias ensure a secure solder joint for the thermal pad and prevent solder from floating the package during assembly, which could hamper forming good solder joints at the QFN contacts.
- An assembly shop can compensate for a lack of through vias in a thermal pad by adding windowpane-shaped opening in the solder paste stencil above the pad, to relieve solder pooling and outgassing during assembly, but the fix is less effective than if vias were present.
- Check for minimum clearance of traces and vias from the routed/scored edges.
- Check the position of vias for BGA packages.
- Via-in-pad design requires filling.
- Dog-bone design: Separate each via from its pad with a predefined short trace covered with solder mask. Ensure there is no mask clearance for the vias under BGA.
- The board documentation should include a drill file with tool codes and X-Y coordinates for all holes.
- The fab drawing should include a drill chart with hole symbols on the drawing and finished hole sizes along with via tolerances.
- The Gerber files should include via plugging holes if required.
- Controlled depth for blind and buried vias.
- Tolerance:

    - o Minimum outer layer annular ring: as per IPC standards
    - o Minimum inner layer annular ring: as per IPC standards
    - o Drill to plane clearance: 8 mils
    - o Diameter: ± 3 mils preferred
    - o Location: 1 mil
    - o Registration: 1 mil
    - o Via clearance of solder mask: 2.5 mils bigger than via pad size
    - o Encroachment of solder mask onto via: via size + 3 mils
    - o Anti-pad: 16 mils bigger than the hole size and plane relief preferred 8 mils

There may be requirements for fabricators to plug, fill, or tent vias on a PCB.

7.4.3 Via Design

The effects of via design are discussed in this section. The Via design depends on two parameters: the drill size and the pad size/annular ring. These parameters are recommended in IPC standards.

The drill size depends on the thickness of the board. In a power board requiring high currents, the drill size will depend on the current required per via.

7.4.3.1. Class Type and Minimum Drill and Pad Requirements

The charts mentioned below show that for a class 2 62 mil PCB the recommended drill size is 8 mils with a pad size of 18mils. For class 3 62 mils PCB the recommended drill size is 8 mils and pad size is 23 mils.

- Depending upon the Performance, the designs are classified as follows:

    1. Class-1: General electronic products
    2. Class-2: Dedicated service electronic products
    3. Class-3: High reliability electronic products

- Drill values depend on the class of the design, fabrication technique, and the PCB thickness.

Below given are the few values for Class-2 and Class-3 that should be followed.

	Drill	Pad	Anti-Pad	PCB Thickness	Aspect Ratio
	0.006"	0.016"	0.026"	up to 0.039"	6.5:1
Drill & Pad Diameter	0.008"	0.018"	0.028"	up to 0.062"	7.75:1
IPC Class 2	0.010"	0.020"	0.030"	up to 0.100"	10:01
1/2 oz copper	0.012"	0.022"	0.032"	up to 0.120"	10:01
	0.0135"	0.024"	0.034"	up to 0.135"	10:01

	Drill	Pad	Anti-Pad	PCB Thickness	Aspect Ratio
Drill & Pad Diameter	0.008"	0.023"	0.033"	up to 0.062"	7.75:1
IPC Class 3	0.010"	0.025"	0.035"	up to 0.100"	10:01
1/2 oz copper	0.012"	0.027"	0.037"	up to 0.120"	10:01
	0.0135"	0.028"	0.038"	up to 0.135"	10:01

Drill & Pad Diameter	8 Layers or less	>8Layers			
IPC Class 2	Pad dia over drill	Pad dia over drill			
1/4 oz copper	0.010"	0.010"			
3/8 oz copper	0.010"	0.010"			
1/2 oz copper	0.010"	0.010"			
1 oz copper	0.012"	0.012"			
2 oz copper	0.014"	0.014"			
3 oz copper	0.016"	0.016"			
4 oz copper	0.018"	0.018"			

Drill & Pad Diameter	8 Layers or less	>8Layers	Drill & Pad Diame	8 Layers or less	>8Layers
IPC Class 3	Pad dia over drill	Pad dia over drill	IPC Class 3A	Pad dia over drill	Pad dia over drill
1/4 oz copper	0.013"	0.015"			
3/8 oz copper	0.013"	0.015"			
1/2 oz copper	0.013"	0.015"	1/2 oz copper	0.013"	0.015"
1 oz copper	0.015"	0.017"	1 oz copper	0.015"	0.017"
2 oz copper	0.016"	0.018"	2 oz copper	0.016"	0.018"
3 oz copper	0.019"	0.021"			
4 oz copper	0.022"	0.024"			

7.4.3.2 Current carrying capacity of Vias

Vias are often used to tie power planes together and therefore it becomes necessary to know the current capacity of the via. To understand the current capacity of a via, it's necessary to know the surface area of the via. The via forms a cylinder in the via drill hole. The length of the cylinder is the thickness of the board 'B'. The surface area of the cylinder formed by the via copper plating 'p' is given by p*D* B where D is the drill size or diameter of the drill hole. The thickness of the cylinder is equal to the plating thickness which is 0.8 mils. If the cylinder of the via is imaginarily cut along its length B and spread out, the via cylinder will be a trace of length B, thickness t=0.8 mils, and width p*D = 3.14 * via drill size. For 8 mils dril,l the trace width would be 8*3.14 = 25.12. Using a standard trace current calculator with ambient of 25 ºC and temperature rise of 5 degrees and since the via is not covered by solder its equivalent to an external trace. For an 8 mil drill the current capacity for 5 ºC temperature rise is 0.8 amps.

Inputs:

Current	0.85	Amps
Thickness	0.8	mil

Optional Inputs:

Temperature Rise	5	Deg C
Ambient Temperature	25	Deg C
Trace Length	1	inch

Results for Internal Layers:

Required Trace Width	64.5	mil
Resistance	0.0132	Ohms
Voltage Drop	0.0112	Volts
Power Loss	0.00955	Watts

Results for External Layers in Air:

Required Trace Width	24.8	mil
Resistance	0.0344	Ohms
Voltage Drop	0.0292	Volts
Power Loss	0.0249	Watts

Table 1: Current calculator for trace width

Drill size	Equivalent trace mils	Current A
8	25.12	0.8
10	31.4	1
12	37.68	1.15
14	43.96	1.25
16	50.24	1.4
18	56.52	1.55
20	62.8	1.65
22	69.08	1.8
24	75.36	1.9

Table 2: Drill size and current capacity

7.4.4 Microvias Design

Microvias are the holes with diameters less than 6 mils. Practically speaking, vias possess an inductive and capacitive parasitic value. The smaller vias have lower capacitance whereas the short length, larger diameter vias have lower inductance. The inductive and capacitive parasitics will affect the high-speed signals.

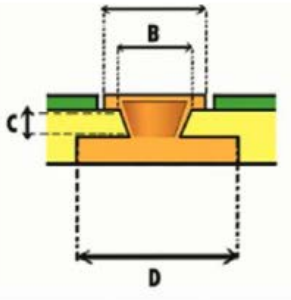
The designer should use the upper layers for high priority supplies. Placing high transient current supplies vertically closer to the device decreases the distance the currents need to propagate through the vias. Also, the ground planes should be adjacent to high transient current power planes to reduce inductance and couple the high-frequency noise.

The most important thing to consider while incorporating vias is the aspect ratio. The aspect ratio, via diameter to the dielectric thickness of the spanned layer, decides the reliability of a PCB. To understand more about vias, please have a look at Sierra Circuits' DFM Handbook.

ASPECT RATIO OF LASER-DRILL MICROVIAS

- RATIO OF LASER MICROVIA = C/B:1
- MOST PRODUCTIVE AND COST-EFFECTIVE A?R IS .75:1 OR LESS

Microvia Hole Diameter	Maximum Dielectric Layer Thickness (mils)			
	A/R =0.5	A/R =0.75	A/R =0.9	A/R =1
6.00	3.0	4.50	5.40	6.00
5.00	2.5	3.75	4.50	5.00
4.00	2.0	3.00	3.60	4.00
3.00	1.5	2.25	2.70	3.00
2.00	1.0	1.50	1.80	2.00



8. Appendix

8.1 High-Speed PCB Design Checklist

There are plenty of things that a designer should remember while designing a PCB. Just so that you don't miss out the vital aspects of designing, keep this checklist right by your side when you draft your design.

1. Layout related:
    a. Verify that high-speed traces do not cross broken planes and are routed on solid planes.
    b. Controlled impedance traces should have ground reference for top and bottom layers.
    c. Controlled impedance traces should have ground reference on both sides in inner signal layers.
    d. Ground and power vias are near the related component pad with very short traces.
    e. Keep ground current loops minimum.
    f. Mention controlled impedance traces in your fab notes.
2. Mark the dimensions of the board.
3. Hole to hole dimension and mounting hole dimension start from the edge of the board.
4. Label all the test points.
5. Include signal names for connector pins wherever possible.
6. All legend text should be aligned in one or two directions only (size 30/6mils nom 25/4).
7. All polarized components should possess polarity marking.
8. All ICs must have pin 1 indication.
9. Fab drawing checklist:
    a. Fab notes:
        i. IPC Class 2 or Class 3 board type
        ii. Layer wise impedance track details
        iii. Color of solder mask
        iv. Annular ring/drill size (minimum)
    b. Layer stack-up:
        i. Mark board thickness
        ii. Copper thickness for every layer
        iii. Insulation material name and thickness
        iv. Mention notes for blind and buried vias if applicable
        v. Add a note for filled via-in-pads for BGA
        vi. Fiducials minimum 3
10. Check if all the SMD components have defined solder mask and solder paste.
11. Verify whether the through-hole components have solder mask openings.

12. The exposed center pad of QFN ICs should have paste in small patches.
13. Update the drill chart.
14. The drill chart should have separate drill symbols for each drill size:
    a. Use “+” for vias
    b. Square with an alphabet for plated holes (PTH)
    c. Triangle with an alphabet for non-plated holes (NPTH)
15. Drill chart should display:
    a. +/– 3 mils tolerance for PTH
    b. +/ – 2 mils tolerance for NPTH
    c. Tolerance on vias can be adjusted depending on the via drill and pad size
    d. Typical via tolerance is set to +/– 3 mils
    e. Check if all the drills (in the drill chart) are whole numbers
    f. Check if each drill matches the desired value
16. Check the dates and verify the date format in the template.
17. Check the layout design file name.
18. Update the name of the design in the template block.
19. Check and clear all valid DRCs.
20. Routing should be 100%.
21. Read all the notes mentioned in the fab layer and other layers. Any changes made should be updated immediately. Also check the impedance value with layer stack.
22. Create Gerber files.
23. View the files with GC Prevue:
    a. Inspect for cleanliness, absence of silvers, and hanging nets
    b. SMB and SPB match
    c. SMT and SPT match
24. Using GC Prevue, inspect individual copper pours for minimum spacing and absence of shorts between different copper pours.
25. BOM validation with the right part numbers
26. Create documents on:
    a. Assembly top and bottom layers
    b. Fab drawing
    c. Drill drawing
    d. All layers
    e. Schematic PDF
27. Cutout on the board:
    a. Mark cutout on the board outline layer and fab layer
    b. Marking with dimensions on fab layer
    c. When generating Gerbers enable board outline layer on all layers
    d. Verify it in all layers by opening the Gerbers
    e. Cutout outline layer must be 2 mils
28. Select the appropriate files (All .art files, art_aper, art_param, nc_param, .drl, placement file, ipc file).

These pointers will definitely assist a designer to craft a board that can be easily manufactured.

8.2 Sierra Circuits Deliverables

The Design deliverable in form of soft files will include the following:

- Gerbers:
    - TOP - top layer
    - SMT - solder mask top
    - SPT - solder paste top
    - BOT - bottom layer
    - SMB - solder mask bottom
    - SPB - solder paste bottom
    - SST - silkscreen top
    - SSB - silkscreen bottom
    - AST - assembly top
    - ASB - assembly bottom
    - Inner layers signal and power /GND
- FAB drawing Outline drill drawing
- NC drill file
- Pick and place file
- IPC 356 netlist file
- ODB++ file
- Project files (on request) CAD Files

8.3 Sierra Circuits PCB Design Capabilities

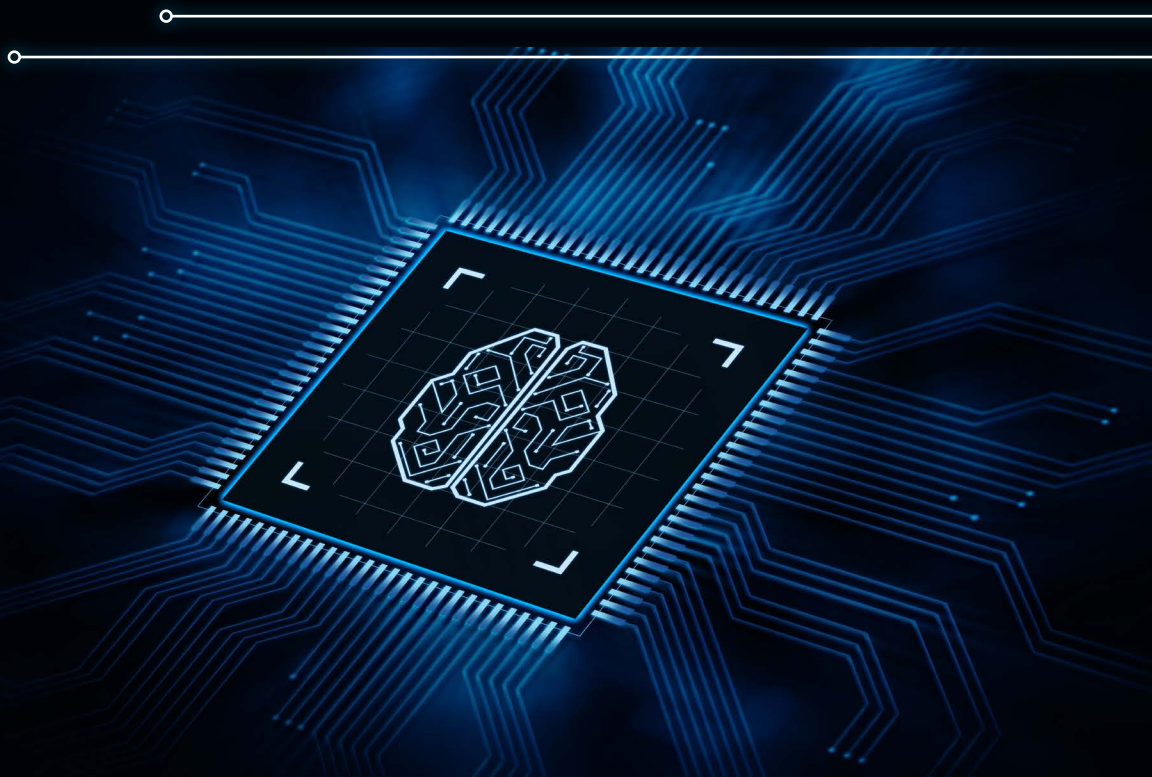
- High-speed digital designs, analog designs, mixed designs, power designs, and RF designs
- PCB design with controlled impedance requirements
- PCB design for mechanical-constrained boards and enclosures
- PCB design for flex, rigid and rigid-flex designs
- PCB designs for mobile phones
- HDI designs with via-in-pad, blind via, buried via and micro vias, via stacking and staggering technology
- Designs with fine pitch BGAs of 0.4mm and 0.5mm
- Designs with high-pin count full matrix BGAs 0.4mm pitch, PoP package, with 2 mil/ 2mil tracks/spacings
- Design for ROHS compliance
- Stack-up design and impedance calculation for single-ended, differential, and co-planar-waveguide models

https://www.protoexpress.com/pcb/pcb-design-service/

A Special Thank You to Anil S Raiker

This book couldn't have been put together without the guidance of our beloved PCB Design Head, Mr. Anil. S. Raiker. Anil has an industry experience of more than 30 years and has a strong academic background with two master's degrees. He is quite passionate about PCB designing and leads some of the finest designers in the industry. Anil is a thinker, innovator, and a well-established PCB designer. He finds satisfaction in solving complex problems and never stops updating himself with new technologies. Apart from designing, Anil loves to explore new places in his free time. We are glad to have him on board. Thank you, Anil!

SIERRA CIRCUITS



Sierra Circuits
1108 West Evelyn Avenue
Sunnyvale, CA 94086
+1 (408) 735-7137

www.protoexpress.com