WELLY NET v00.1

SOFTWARE

- Devices MUST start communications with an 8 bit destination address
- Devices MUST NOT use 0 and 255 addresses
- Devices MUST NOT attempt communications if the transmit activity line is high (do not disturb sign)
- Devices MUST have a random back off (1-10ms)
- Devices MUST communicate at 9600 bits per second (bps)
- All devices MUST receive and interpret data addressed to 0x00
- Devices MUST receive and interpret data sent to their addresses
- Devices MAY receive and interpret data addressed to 255
- Messages beginning with ASCII « E » SHALL BE interpreted as an event
- Messages beginning with ASCII « A » SHALL BE interpreted as an instruction
- Messages length SHALL BE transmitted as the 3rd bit of Header
- Messages length SHALL represent the length of the message after Header
- Messages MAY have a payload of up to 253 bits

HARDWARE

- Devices MUST use a 5V TTL (Transistor to Transistor Level)
- Devices MAY draw up to 5mA
- All devices with on-board regulation MUST NOT connect the VCC line to the on-board VCC (if devices requires on-board regulations, can use optical isolation)
- Unused pins on the Header MUST BE put in a High impedance state
- The bus MUST BE supplied with a stable 5V supply of at least 2A

RFC2119 : specifications guidelines
MUST/MUST NOT: required
SHOULD/SHOULD NOT: recommended
MAY: suggested

NOTES
Any digital line on the ATtiny can be used
Header: Dest | Send | Length
NC: non-connected
DND: do not disturb
Rx → TLK (Talk): MISO
Tx → NC: MOSI

TO DO LIST

- Reference implementation board
- Create our library
- Create code list